The Dissertation Committee for Hyejeong Song
certifies that this is the approved version of the following dissertation:

PLL-Based Digitally-Intensive Wireless Transmitter Architectures Employing RF Pulse-Width Modulation

Committee:

Ranjit Gharpurey, Supervisor

Jacob A. Abraham

Deji Akinwande

Michael Orshansky

Lei Ding

PLL-Based Digitally-Intensive Wireless Transmitter Architectures Employing RF Pulse-Width Modulation

by

Hyejeong Song, B.S., M.S.

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To my beloved family

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PLL-Based Digitally-Intensive Wireless Transmitter Architectures Employing RF Pulse-Width Modulation

Hyejeong Song, Ph.D.
The University of Texas at Austin, 2017

Supervisor: Ranjit Gharpurey

3G and 4G wireless networks have been recently proposed for Machine to Machine (M2M) communications in order to achieve ubiquitous coverage, robust security and high reliability. The most critical design consideration in transceivers for several portable Internet of Things (IoT) wireless communication applications is often power efficiency. This poses a key design challenge in wireless transmitters for communication standards that utilize high peak-to average power ratio (PAPR) signals.

In this work, two PLL-based digitally-intensive wireless transmitter architectures employing RF-Pulse Width Modulation (RF-PWM) are presented, in order to address the efficiency challenge. The first architecture employs envelope and phase information, while the second utilizes quadrature I-Q signal components directly. A key contribution of this work is the use of analog-domain Pulse-Width Modulation (PWM) that can directly generate the output signals at the desired RF band without the need for frequency

up-conversion and without degradation caused by quantization. By employing Class-D output stages, the proposed architectures can provide enhanced efficiency and allow for the use of broadband loads. These approaches make the designs suitable for multi-band and multi-mode operation. Furthermore, the digitally-intensive architectures can benefit from technology scaling.

A prototype RF-PWM transmitter with a Class-D power amplifier (PA) which utilizes a polar approach is implemented in a 65-nm CMOS technology. For an LTE signal with a 1.4 MHz bandwidth and a 6.4 dB peak-to-average-power ratio (PAPR), the RF-PWM transmitter achieves a power-added efficiency (PAE) of 17.5% and an adjacent channel leakage ratio (ACLR) of -30.9 dBc and -31.1 dBc at an average output power of 16.1 dBm. The proposed transmitter achieves a peak output power of 22.4 dBm with 46.6% PAE and 38.8% efficiency for the full RF-PWM transmitter, including PAs.

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[1]Part of the material in this chapter is based on [1] which has been published in IEEE Radio Frequency Integrated Circuits Symposium, 2015. The author Hyejeong Song was responsible for the design, implementation and measurement of the transmitter IC described in the paper.

[2]Part of the material in this chapter is based on [2] which has been published in IEEE DCAS 2016. The author Hyejeong Song designed and simulated the architecture.

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Chapter 1

Introduction

Over the past three decades the number of mobile devices that employ wireless communications, such as smart phones, tablets and portable computers has grown to several billions. With the proliferation of IoT-based applications, (Fig. 1.1), relating to smart-grid, security, health monitoring and transportation, the demand for wireless communications is expected to increase even more rapidly over the next decade.

Many of these systems require data rates in the order of Mbps or more. Since these systems operate in bandwidth-constrained environments, supporting these data rates often implies the use of signals with high peak-to-average ratios (PAPRs). Linear power amplifiers (PAs) are widely used for such RF transmitter implementations. These PAs provide good linearity, although often at the expense of efficiency. Also, the efficiency of linear PAs degrades rapidly as the output power is reduced (back-off mode). As such, these are not well-suited for applications that employ modulation schemes with a large PAPR.

Switch-mode PA topologies offer a promising alternative for such systems which employ modulation schemes with large PAPR due to their in-

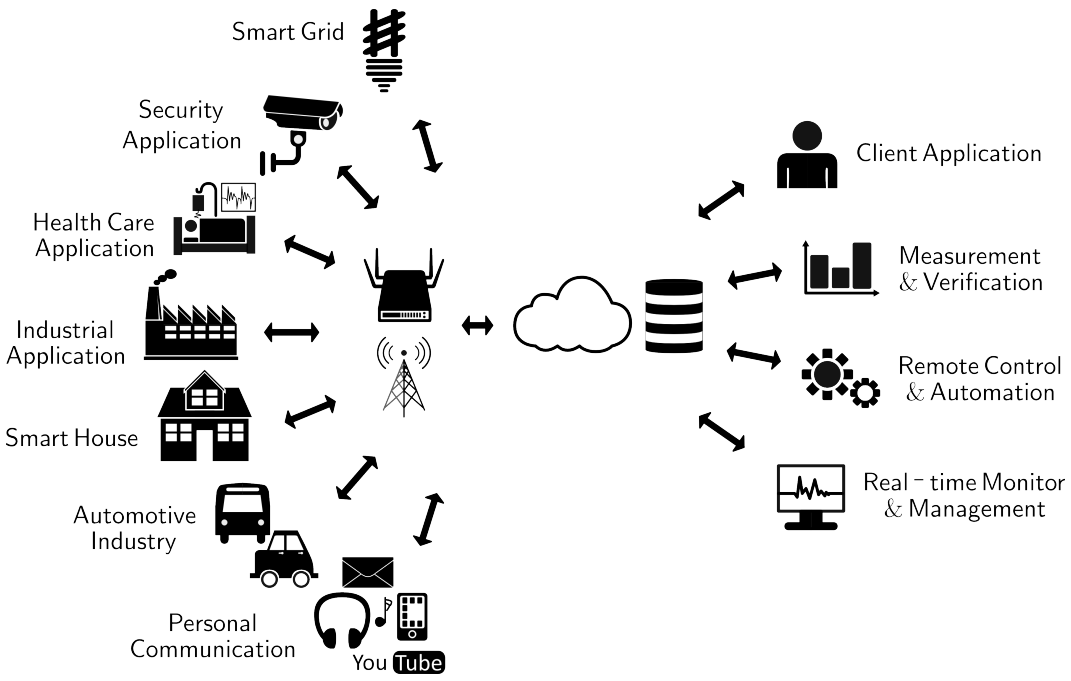


Figure 1.1: Potential applications of the Internet of Things

herently high efficiency. Switch-based PA implementations also allow for utilization of deep submicron CMOS technologies. This enables single-chip SoC implementations that integrate RF PAs along with digital baseband and application processors, which can reduce cost and size. The high-performance, deep-submicron CMOS technologies can help to lower cost and make possible a greater level of integration, which is critical for enabling the proliferation and mass deployment of these communication devices.

Several modulation techniques can be used to drive switch-mode PAs. Pulse-width modulation (PWM) encodes signal amplitude information in the duty-cycle of a periodic pulse waveform. It typically employs two-level signaling and can hence be easily utilized with switch-mode PAs. A different form of PWM, namely radio frequency pulse-width modulation (RF-PWM), encodes envelope information in the pulse duty cycle, and phase information in the pulse position [3, 4, 2, 1, 5]. Another form of modulation that has been demonstrated along with switching stages for wireless applications is sigma-delta modulation [6]. Continuous-time RF-PWM, and PWM offer a key advantage compared to sigma-delta modulation, in that these schemes inherently lack quantization noise. Spurious information is localized near harmonics of the carrier, where it can be attenuated by employing low-complexity filters.

There are several architectural options for converting signals in PWM. In [7] a baseband sigma-delta modulator is employed for providing digital I-Q PWM and combined with a digital upconverter. In [8], baseband PWM is generated using a VCO-based opamp and is upconverted using an LO in an

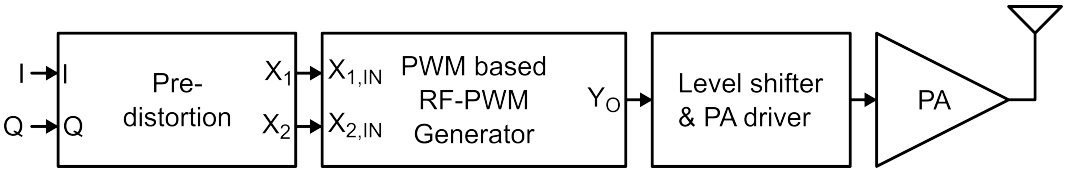


Figure 1.2: The proposed RF-PWM transmitter

RF DAC for a wireless transmitter application. In [9], RF-PWM is generated by two out-phased signals.

The work presented in this thesis proposes two architectures for high-efficiency wireless transmitters that seek to enhance power efficiency and reconfigurability (Fig. 1.2). The first approach is a polar RF-PWM transmitter which is controlled by the envelope and phase information of the input signal, while the second approach is a Cartesian RF-PWM transmitter which uses quadrature I/Q input signal components. Key to both architectures is the use of PWM signaling, which is generated in the analog-domain, and hence can avoid quantization noise. Furthermore, these techniques can directly generate the output signals at the desired RF band without any need for frequency up-conversion. The pulse-width modulator can drive a Class-D output stage which allows for the use of a broadband load. This makes the design a candidate for reconfigurable radio transmitters that can operate over a wide frequency-range.

In addition, a general model of the proposed PLL-based RF-PWM is derived, which allows for noise analysis of the proposed architectures. The analysis is useful for predicting both in-band noise, which is a critical consid-

eration for ensuring that the spectral mask is satisfied, and out-of-band noise, which needs to be sufficiently low such that it does not degrade the sensitivity of a receiver stage in another transceiver.

A prototype of the PLL-based RF-PWM transmitter with a Class-D PA is implemented in a 65-nm CMOS technology. The RF-PWM transmitter, including Class-D PAs, achieves a peak output power of 22.4 dBm with 46.6% power-added efficiency (PAE) and 38.8% peak total efficiency, at 2.66-GHz.

This dissertation is organized as follows. Chapter 2 describes the fundamentals of radio transmitters including Cartesian architectures, PAs, and linearization techniques for RF transmitters employing switch-mode PAs. In Chapter 3, the PLL-based PWM architecture is introduced and analyzed in the frequency domain by using a linear model. In Chapter 4, a digitally-intensive RF transmitter employing RF-PWM which is implemented in a 65-nm CMOS technology is proposed. The architecture and key design blocks are discussed. Further, a noise analysis of the RF-PWM system is provided employing a linear model. The measurement set-up and the results are described. In Chapter 5, a Cartesian 3-level RF-PWM CMOS transmitter is proposed and analyzed by using a linear model. Conclusions and suggestions for future work are provided in Chapter 6.

Chapter 2

Transmitter Architectures

A conventional direct conversion Cartesian transmitter, which consists of a digital signal processor (DSP), digital to analog converters (DACs), low pass filters (LPFs), up-converters, PA driver, and PA, is shown in Fig. 2.1. It utilizes quadrature I and Q signal components to represent the complex baseband symbols. A large fraction of the power dissipation in transmitters is often observed in the output stage, which includes the PA driver and the PA, and as such the efficiency of these output stage designs is critical in determining the overall transmitter efficiency. In this chapter, existing techniques for implementation of high-efficiency transmitters are described.

2.1 Switch-Mode Power Amplifiers

There are two general types of power amplifiers. Linear PAs such as Class-A/-B/-AB/-C designs utilize transistors as voltage-controlled current sources. Their output preserves both the envelope and phase information. The other type consists of switch-mode PAs, such as a Class-D/-E/-F PAs, which utilize transistors as switches and whose output contains only phase information.

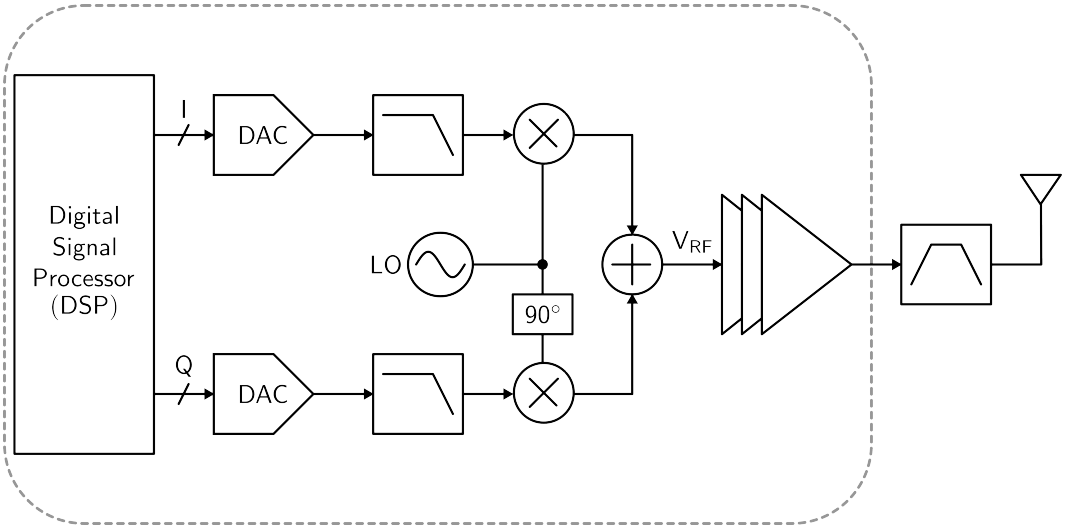


Figure 2.1: A conventional direct conversion Cartesian transmitter

Switch-mode PAs in theory have 100% efficiency, if the loss in the switching transistor is zero [10]. In a practical implementation, multiple factors contribute to reduction of efficiency, such as the ON resistance (R_{ON}) of the transistor, and finite switching time due to parasitic capacitance, which causes the device current and voltage across the device to be simultaneously non-zero. Even in the presence of these non-idealities, switch-mode PAs provide better peak and back-off efficiency than linear PAs (Fig. 2.2).

A Class-D PA (Fig. 2.3a) is an ideal inverter which consists of PMOS and NMOS device pairs [11]. The load is connected to the inverter through a filter and a matching network, which allows for power flow only at the fundamental frequency. Ideally when a device turns on, the voltage across it is zero, which implies that the power dissipation in the device is zero as well, thereby enabling 100% efficiency. In theory, the zero-voltage switching

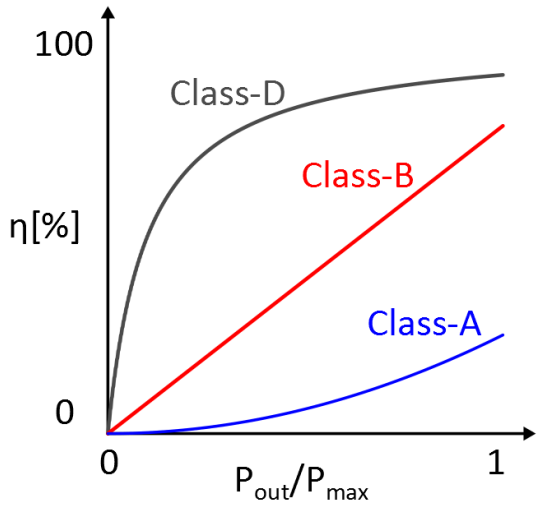


Figure 2.2: Normalized output power vs. the drain efficiency

condition of Class-D PA can be maintained with non-periodic or quasi-periodic driving signals, such as pulse-density or pulse-width modulated signals.

A Class-E PA (Fig. 2.3b) is a switch-mode amplifier with a matching network that is tuned at the fundamental frequency. The matching network is designed to provide zero-voltage switching, and hence the Class-E stages can ideally provide 100% efficiency. Compared to a Class-D PA, only one transistor is used and the impact of parasitic capacitance is smaller. There is no overlap between current and voltage because the drain voltage does not begin to increase until the switching of the device is completed. The conduction angle, supply voltage, and peak current determine the characteristics of a Class-E PA [12]. With the tuned matching network at the output, the peak voltage can be more than three times the supply voltage. This can limit the usable supply voltage, if the transistors cannot support the high peak voltage

levels, which in turn can reduce the output power.

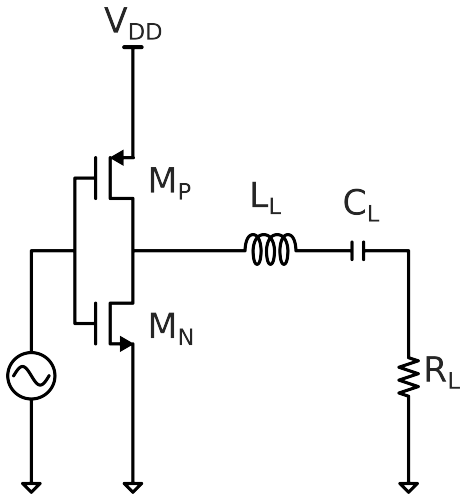
Since switch-mode PAs have only phase information in their outputs, linearization or amplitude restoration techniques are needed for a general signal that has both amplitude and phase variation.

2.2 Linearization Techniques for RF Transmitters Employing Switch-Mode PAs

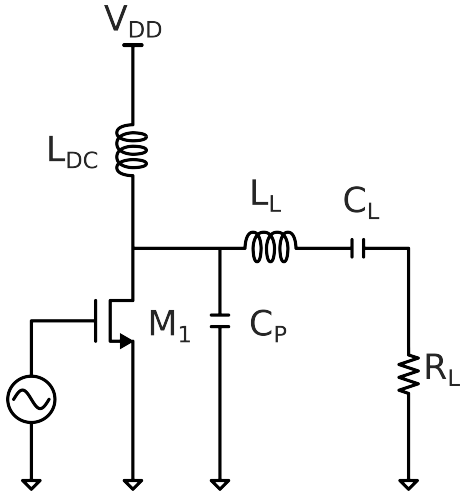
2.2.1 Polar Modulation

A switch-mode PA can support polar modulation, if the power supply of the PA is modulated in response to the envelope information of the signal (Fig. 2.4) [13, 14]. The approach provides enhanced power efficiency at small output power levels because DC power consumption can be optimized through power supply modulation. Key challenges in this approach include the requirement for a high-bandwidth power-supply modulator, which is made even more challenging due to bandwidth expansion inherent to a polar representation, and synchronization between the AM and PM paths e.g., [15].

Kahn Envelope Elimination and Restoration (EER), introduced in [16], is an early example of a polar transmitter implementation which modulates envelope and phase information separately and then combines the two paths at the output stage. A related implementation, which is well-suited for deep-submicron CMOS technology, employs wideband all-digital phase lock loops (ADPLL) for phase modulation, and a digitally-controlled power amplifier (DPA) for amplitude modulation [17, 18]. This approach has been utilized for



(a) Class-D PA



(b) Class-E PA

Figure 2.3: The switch-mode PA designs

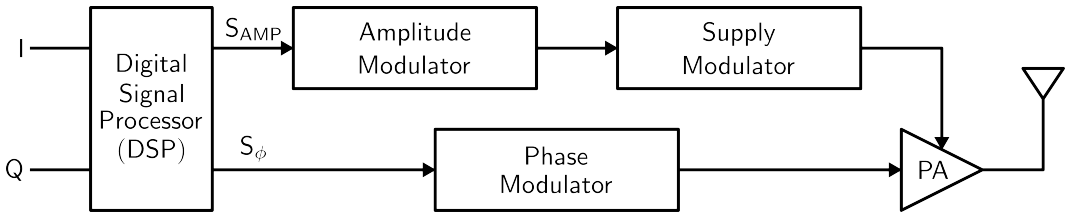


Figure 2.4: Polar modulation

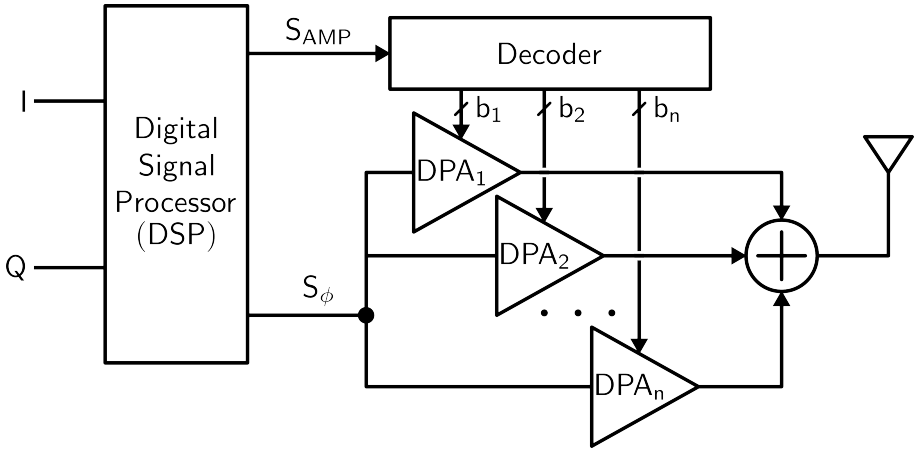


Figure 2.5: Unit-cell based digital power amplifier

IoT applications like Bluetooth Low Energy (BLE) radio [19, 20].

2.2.2 Digital Power Amplifiers

In this approach, amplitude information is derived by using unit digital switch-based amplifiers [21, 22, 23], and varying the number of units in response to the amplitude signal, similar to a current-steering DAC [24]. The approach requires additional linearization techniques like digital pre-distortion (DPD) because of amplitude-dependent impedance modulation at the output. The output resistance of the DPA is signal dependent, which causes the output

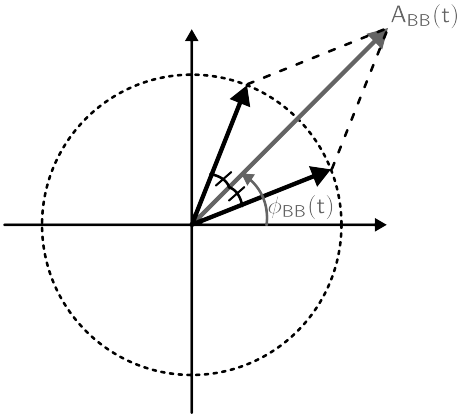
resistance to be modulated when the transistor operating point is modified by a large output voltage swing [25]. This can lead to distortion. In [23, 26], a switched-capacitor PA was introduced as a solution for the impedance variation at the output.

2.2.3 Outphasing Modulation

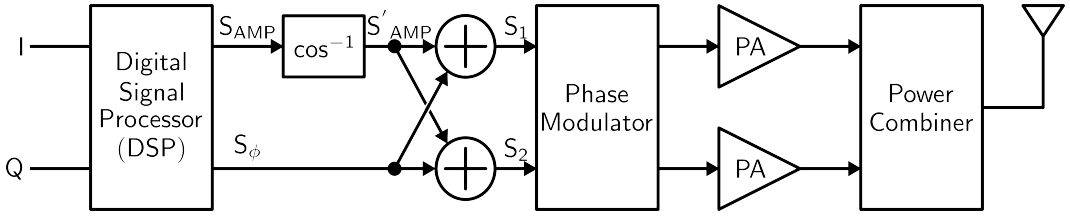
An amplitude and phase modulated signal can be decomposed into two constant amplitude signals with interdependent, time-varying phase information. Outphasing modulation employs this principle. As shown in Fig. 2.6, the desired input signal ($A_{BB}(t)\angle\phi_{BB}(t)$) is expressed by the sum of two vectors (S_{ϕ_1} and S_{ϕ_2}) with constant envelope and phase modulation ($\phi_{BB}(t) \pm \phi_0$) [9, 27, 28, 29, 30, 31]. The two signals $S_{\phi_1}$and S_{ϕ_2} are then used to drive two switch-mode PAs through separate paths. The original signal is recovered by combining the outputs of the two PAs. This scheme requires a passive, low-loss power combining network at the output, which can pose a design challenge.

2.2.4 Pulse Modulation

Pulse modulation encodes amplitude information using a discrete-level pulse waveform. In [6], the baseband signal is converted into a 1-bit signal by using bandpass delta-sigma modulation (BPDSM). This approach requires filtering of out-of-band quantization noise that arises from noise-shaping. Also, there is inherent quantization noise due to digitized amplitude modulation. Another technique introduced in [32] uses digital I-Q PWM signals generated



(a) Two outphased signals derived from the original input signal ($=A_{BB}(t)\angle\phi_{BB}(t)$)



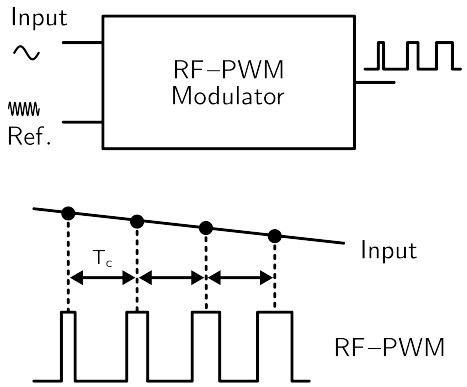
(b) Diagram of outphasing transmitter

Figure 2.6: Outphasing transmitter

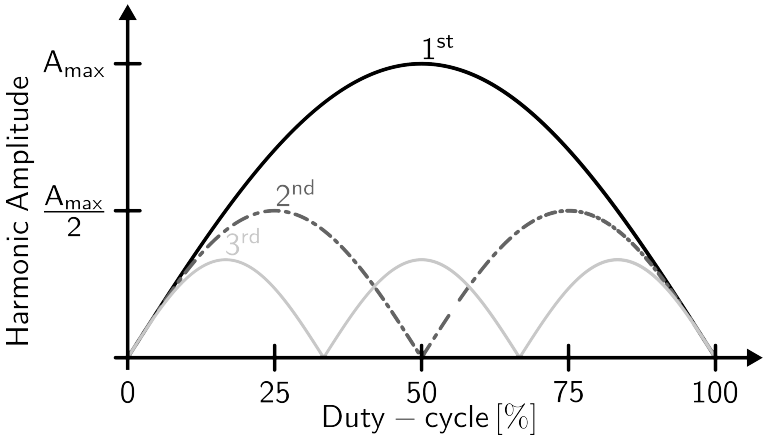
by a baseband delta-sigma modulator (DSM), which are then combined using a digital upconverter. In [33, 34], the noise-shaped signal generated by a DSM is encoded as a binary code at the RF carrier frequency, by using pulse density modulation (PDM), which drives the switch-mode PA. In [8], multiphase PWM is upconverted with an LO carrier signal, which drives an RF DAC.

Radio frequency pulse width modulation (RF-PWM) encodes amplitude information in the duty cycle of a pulse waveform, and phase information in the pulse position [1, 2, 3, 4, 5, 35]. As shown in Fig. 2.7a, RF-PWM generates a pulse signal which controls the pulse width nearly symmetrically around the center of the pulse. The distance between the centers of the pulses is nearly fixed, and is close to the period (T_c) of the carrier frequency, when the carrier frequency is much greater than the signal bandwidth. The relationship between the amplitude of the harmonics of an RF-PWM waveform, and the duty cycle of the signal is shown in Fig. 2.7b. Unlike the delta-sigma approach, RF-PWM does not have high out-of-band quantization noise.

In this thesis, a continuous-time RF-PWM based wireless transmitter architecture is proposed. The design goals include high power efficiency, reconfigurability, and compatibility with digital CMOS processes.



(a) RF-PWM generation



(b) Harmonic amplitude of periodic pulse train

Figure 2.7: RF-PWM

Chapter 3

PLL-Based PWM Generation

3.1 Overview of Pulse Width Modulation

3.1.1 Natural Sampling Single Sided PWM (NSPWM)

Pulse Width Modulation (PWM) is a scheme to represent a signal by a pulse train whose local duty cycle is proportional to the signal amplitude. Analog PWM is often employed in audio applications. A typical architecture employed in this application is shown in Fig. 3.1, wherein the input signal is compared to a ramp signal in a high-speed comparator.

A PWM signal generated in response to a sinusoidal input with a fundamental frequency of f_{IN} can be represented by a double Fourier series (DFS), that can be shown to be [36]

$$\begin{aligned} F_{NSPWM}(t) = \; & K \cdot X_{IN}(t) \\ & +2 \sum_{m=1}^{\infty} \frac{1 - J_0(m\pi M) \cdot cos(m\pi)}{m\pi} \cdot sin(m \cdot 2\pi f_c t) \\ & -2 \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\infty} \frac{J_n(m\pi M)}{m\pi} \cdot sin(m \cdot 2\pi f_c + n2\pi f_{IN} - m\pi - \frac{n\pi}{2}) \end{aligned} \tag{3.1}$$

where K ($\in [0:1]$) is the modulation index and J_n is Bessel function of n^{th}

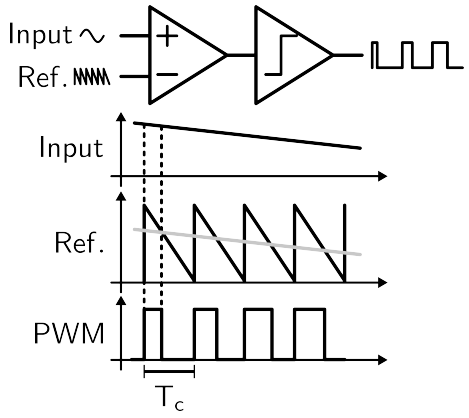
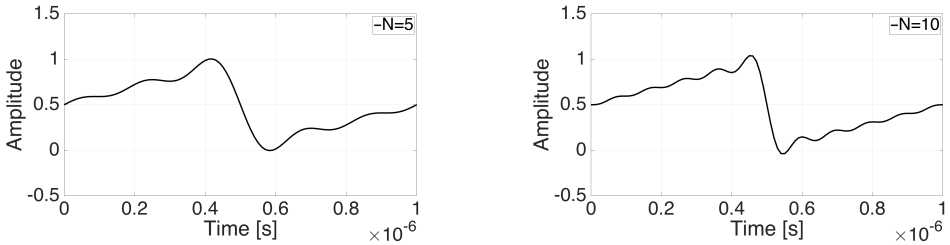


Figure 3.1: Natural sampling left-edge referred PWM

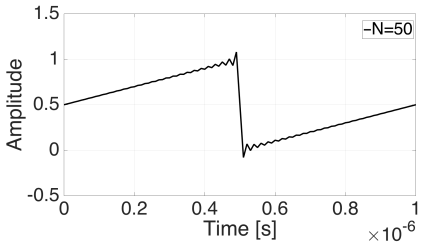
order, n is the index of the harmonics of the input signal frequency (f_{IN}), and m is the index of the harmonics of the carrier frequency (f_c). In Eq. 3.1, the average of the PWM signal is linearly proportional to the input information and there are infinite intermodulation (IM) terms at multiples of ω_{IN} near harmonics of the carrier frequency. The amplitude of the IM terms decreases rapidly due to the scaling factor provided by the Bessel function. For sufficiently large oversampling ratio (OSR), where OSR is given by the ratio ω_c/ω_{IN}, it is possible to minimize degradation of the baseband signal component due to the IM terms.

From Fig. 3.1 and Eq. 3.1, the average of the output PWM signal ($\overline{F_{NSPWM}(t)}$) is given by

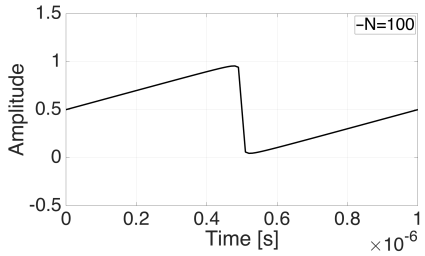


(a) N=5

(b) N=10



(c) N=50



(d) N=100

Figure 3.2: Sawtooth waveform with different number of harmonics

$$\begin{aligned} \overline{F_{NSPWM}(t)} &= \frac{1}{T_c}\int_0^{T_c} F_{NSPWM}(\tau)\,d\tau &&= K \cdot X_{IN}(t) \\ &= \frac{1}{T_c}\int_0^{D(t)\cdot T_c} V_{DD}\,d\tau &&= D(t)\cdot V_{DD} \end{aligned} \tag{3.2}$$

where D is the duty cycle of the pulse and T_c is the period of the carrier frequency (f_c) of the PWM signal. From Eq. 3.2, the duty cycle *(D)* is given by

$$D(t) = \frac{K \cdot X_{IN}(t)}{V_{DD}}. \tag{3.3}$$

3.1.2 Design Challenges for High-Speed PWM Generation

In order to reduce the impact of the IM products on the baseband signal, it is critical to use a high OSR, or alternatively a sufficiently high switching frequency. For signals with bandwidth in the range of several MHz, this can imply the use of periodic ramp waveforms with carrier frequency of the order of GHz. Similar carrier frequencies are also required for RF applications, as described later.

There are several challenges to the use of a comparator-based pulse-width modulator that employs ramp signals at such high frequencies. First, as shown in fig. 3.1, the ideal sawtooth signal that is required for PWM, is given by

$$X_{sawtooth}(t) = \frac{A}{2} - \frac{A}{\pi} \sum_{k=1}^{\infty} (-1)^k \frac{sin(2\pi k \cdot f_{SAW} \cdot t)}{k} \tag{3.4}$$

where A is the amplitude of the sawtooth signal and f_{SAW} is the frequency of the sawtooth signal. The sawtooth signal consists of a sum of infinite harmonics. If the bandwidth of the clock path is limited, this has a significant impact on the shape of the ramp. This is shown in Fig. 3.2, where we assume that the clock path is strictly band-limited to a fixed number of harmonics. As can be observed, the shape of the ramp degrades rapidly, as the number of harmonics is reduced. Since the PWM signal is generated by comparison between the input signal and the sawtooth signal, an imprecise shape of the ramp can degrade the linearity of the system. If the ramp frequency approaches

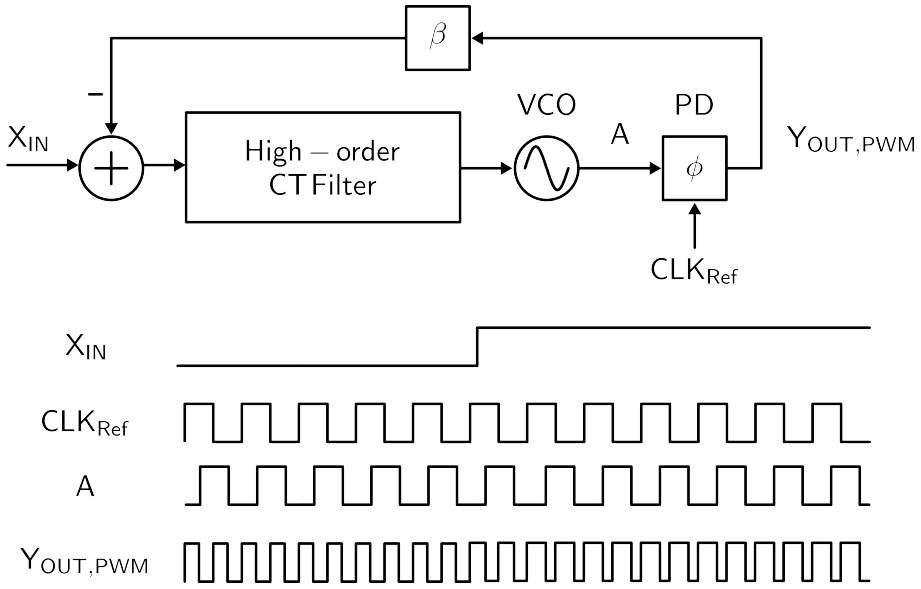


Figure 3.3: PLL-based PWM architecture and associated signals

several hundreds of MHz, it can be observed from Fig. 3.2 that in order to get a precise ramp shape, the clock path needs to have a bandwidth that can be as high as several 10s of GHz.

A second challenge arises from the requirement for a precise comparator that can switch at the ramp rate of the order of GHz, which is very challenging even in advanced silicon technologies.

3.2 PLL-Based PWM Generation

A PLL-based pulse-width modulator is described in [37, 38] and is able to provide PWM signal at RF frequency in the analog domain. As shown in Fig. 3.3, the PLL architecture consists of Voltage Controlled Oscillator (VCO), Phase Detector (PD), and Low Pass Filter (LPF). Unlike a PLL employed in

a wideband frequency synthesizer, which compares the phase of the reference clock signal and the output of VCO, the proposed architecture compares the baseband input information and the output of the PD. The design also employs a negative feedback loop where the error signal is applied to the input of the VCO. The error signal is generated from the average of the difference between the output of the PD and the input signal, and controls the phase of the VCO's output. The phase difference between the VCO output and the reference clock encodes the pulse width of the signal at the output of the PD ($Y_{OUT,PWM}$). When the feedback loop is closed, the error signal is ideally forced to zero, which implies that the average of the output of the PD follows the input information. The output of the PD is a PWM signal with a carrier frequency (f_c) which depends on the frequency of the reference clock ($f_{CLK,Ref}$). In order to generate a PWM signal, a sinusoidal reference is employed instead of a sawtooth signal which avoids the previously described bandwidth requirement of the clock path. Furthermore, the architecture can support multiband operation or be employed in a Software Defined Radio (SDR) since the carrier frequency of the PWM signal can be easily changed by controlling the frequency of the reference clock.

3.3 Analysis of the Proposed PWM Architecture

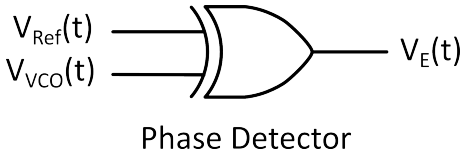
3.3.1 Linear Model of the EX-OR Phase Detector

The EX-OR phase detector generates a signal representing the difference in phase between the VCO output signal and the reference signal (Fig.

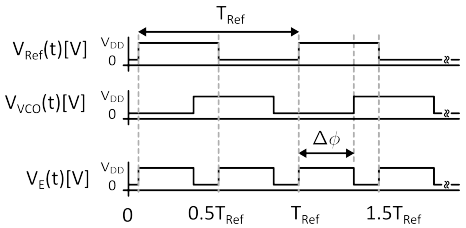
3.4), where $avg.[V_E(t)]$ specifies the average of the phase detector output and $\Delta\phi$ denotes the difference between the phase of the VCO output, ϕ_{VCO}, and the phase of the reference signal, ϕ_{Ref}. As shown in Fig. 3.3, the output of the phase detector is applied to the loop filter and the output of the loop filter is applied to the input of the VCO. The pulse width is the same for both cases (Fig. 3.4b and Fig. 3.4c), however, the gains ($\frac{avg.[V_E(t)]}{\Delta\phi}$) of the phase detector in the two cases are $\frac{V_{DD}}{\pi}$ and $-\frac{V_{DD}}{\pi}$ respectively assuming that the PD output switches between 0 and V_{DD} (Fig. 3.4d). The input of the phase detector should be in the interval where the gain is $-\frac{V_{DD}}{\pi}$ in order to ensure negative feedback in the PWM loop. Phase detection is a memory-less operation and hence can be modeled by a constant gain as noted in [39]. The constant-gain model eases analysis of PLL and PLL-based pulse-width modulators, where the loop-dynamics and overall performance are primarily governed by the baseband frequency response.

3.3.2 Linear Model of PLL-Based Pulse-Width Modulator

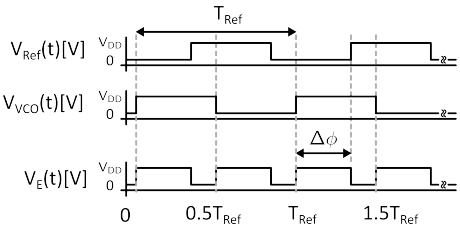
The linear model of the PLL-based pulse-width modulator is shown in Fig. 3.5. The loop shown in Fig. 3.5 is a type-II Phase-Lock Loop (PLL), since it has two integrators in its open-loop transfer function. These are provided by the loop-filter and the VCO. The VCO (H_{VCO}) is modeled as an ideal integrator with the constant gain (K_{VCO}). The phase detector provides a constant gain (H_{PD}) of $-\frac{V_{DD}}{\pi}$, assuming that the PD output has 2-levels (0 and V_{DD}). The frequency response of the operational amplifier is given by



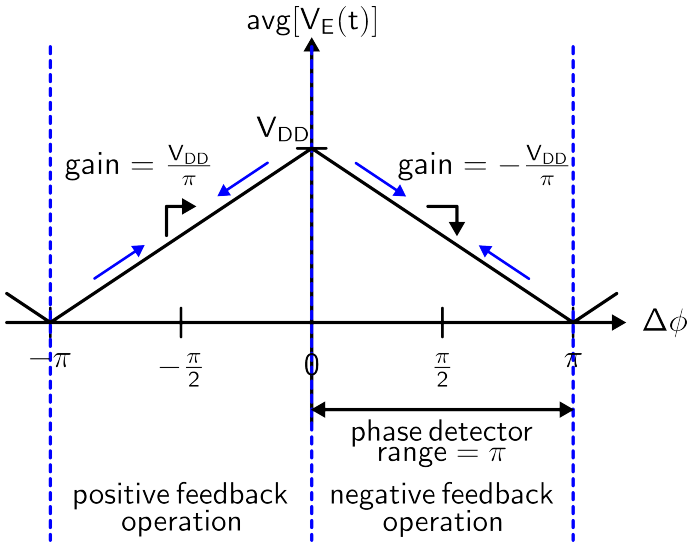
(a) EX-OR phase detector symbol



(b) Leading case ($0 < \Delta\phi < \pi$)



(c) Lagging case ($-\pi < \Delta\phi < 0$)



(d) Operating range of EX-OR phase detector

Figure 3.4: EX-OR phase detector and associated signals

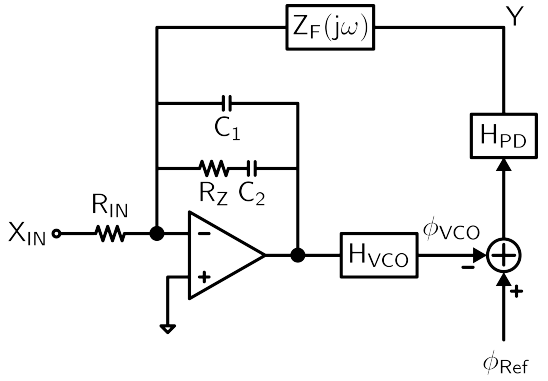


Figure 3.5: Linear model of PLL-based PWM

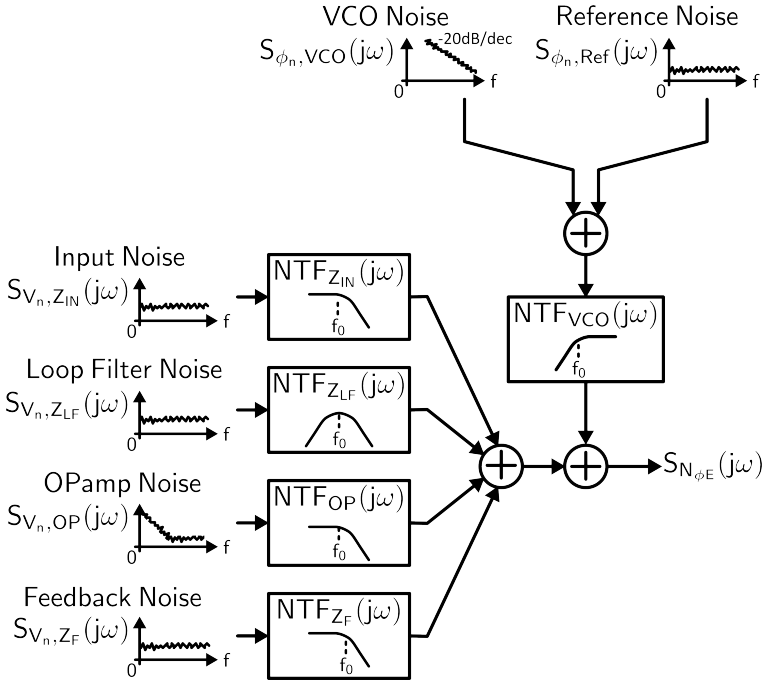


Figure 3.6: PLL noise

$A_{OP}(j\omega)$. Using the above notation, the open-loop gain, $A_{OL}(j\omega)$, and the resulting transfer function, $\phi_E(j\omega)/X_{In}(j\omega)$, can be shown to be given by:

$$A_{OL}(j\omega) = \frac{-A_{OP}(j\omega) \cdot Z_{LF}(j\omega) \cdot H_{VCO}(j\omega) \cdot H_{PD}}{(A_{OP}(j\omega)+1) \cdot Z_F(j\omega) + Z_{LF}(j\omega) \cdot \left\{ \frac{Z_F(j\omega)}{Z_{IN}(j\omega)} + 1 \right\}} \quad (3.5)$$

$$\frac{\phi_E(j\omega)}{X_{IN}(j\omega)} = \frac{A_{OL}(j\omega)}{1 - A_{OL}(j\omega)} \cdot \frac{Z_F(j\omega)/R_{IN}}{H_{PD}} \quad (3.6)$$

where $Z_{IN}(j\omega)$ is the input impedance and $Z_F(j\omega)$ is the feedback impedance. $Z_{LF}(j\omega)$ is the transfer function of the input low-pass filter and is given by $Z_{LF}(j\omega) = 1/(j\omega C_1) \parallel (R_Z + 1/(j\omega C_2))$ [38].

The magnitude response of $\frac{\phi_E(j\omega)}{X_{IN}(j\omega)}$ is shown in Fig. 3.7. The magnitude of $\frac{\phi_E(j\omega)}{X_{IN}(j\omega)}$, from Eq. 3.6, has a constant gain within the signal bandwidth of the input (X_{IN}). Using this result in Eq. 3.3, the coefficient K that relates the duty-cycle (D) to the input (X_{IN}) can be shown to be

$$K = \frac{D \cdot V_{DD}}{X_{IN}} = \frac{T_{Ref}}{2\pi} \cdot \frac{2}{T_{Ref}} \cdot \frac{\phi_E}{X_{IN}}. \quad (3.7)$$

3.3.3 Noise Analysis of the PLL-Based Pulse-Width Modulator

By using the linear noise model shown in Fig. 3.8, the noise transfer function (NTF) from various noise sources to the phase error (ϕ_E) can be shown to be

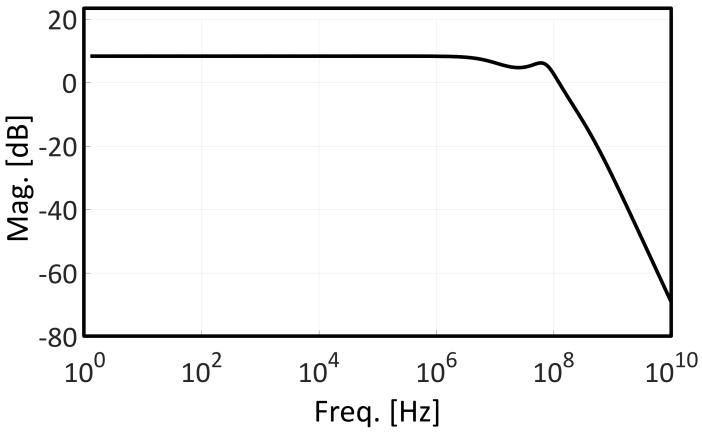
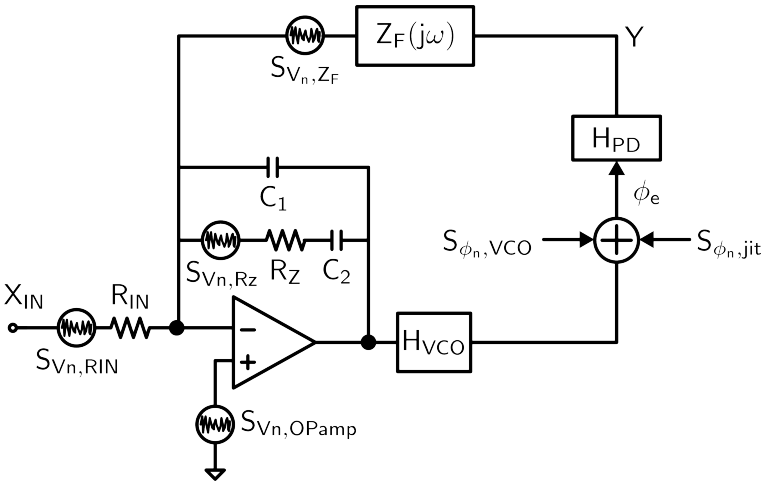


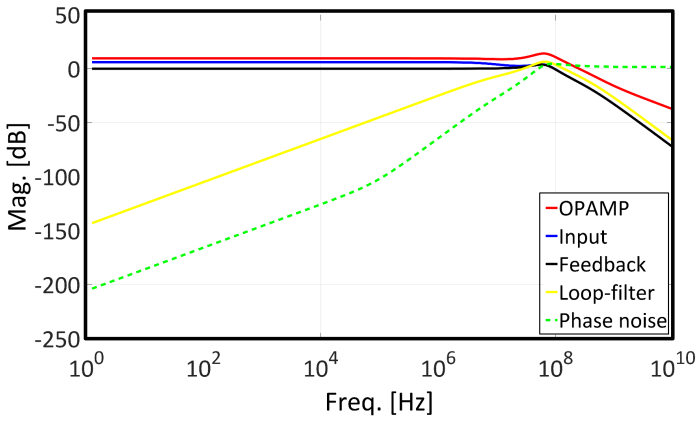
Figure 3.7: Magnitude response of $\phi_E(j\omega)/X_{IN}(j\omega)$

$$
\begin{aligned}
NTF_{VCO}(j\omega) &= \{1 + G(j\omega)\} \\
NTF_{Z_{IN}}(j\omega) &= G(j\omega) \cdot \frac{Z_F(j\omega)/Z_{IN}(j\omega)}{H_{PD}} \\
NTF_{OPAMP}(j\omega) &= -G(j\omega) \cdot \frac{1 + Z_{LF}(j\omega) \cdot \{Z_F(j\omega)/Z_{IN}(j\omega) + 1\}}{Z_{LF}(j\omega) \cdot H_{PD}} \\
NTF_{Z_F}(j\omega) &= G(j\omega) \cdot \frac{Z_F(j\omega)}{R_{RF} \cdot H_{PD}} \\
NTF_{Z_{LF}}(j\omega) &= G(j\omega) \cdot \frac{Z_F(j\omega) \cdot \{j\omega C_2 + R_Z\}}{j\omega C_2 \cdot R_Z \cdot H_{PD}}
\end{aligned}
\tag{3.8}
$$

where $G(j\omega) = A_{OL}(j\omega)/\{1 - A_{OL}(j\omega)\}$. Fig. 3.6 graphically summarizes the frequency response of the NTF and the noise sources that provide a total phase error noise (N_{ϕ_E}). Both VCO noise and reference noise are high-pass filtered by the loop, which results in suppression of both noise sources over a wide frequency range that is related to the system bandwidth. These noise



(a) Linear model with noise sources



(b) The noise transfer function (NTF) from various noise sources to ϕ_E

Figure 3.8: Various noise sources and NTFs

sources, however, still have a significant impact on the out-of-band noise, which can be critical in a wireless system. On the other hand, the noise sources of the analog filter are low-pass filtered and the noise of R-C-C low-pass filter is band-pass filtered by the loop, which affects the in-band noise of phase error noise (N_{ϕ_E}).

3.4 Conclusion

The PLL-based PWM architecture described above can be implemented without a high speed ramp signal and a comparator. It is suitable for generation of PWM signals at high carrier frequencies, because it utilizes a sinusoidal signal as a reference clock instead of a sawtooth signal. It is also capable of supporting multi-band and multi-mode operation. Finally, since it generates the PWM signal in the analog domain, there is no quantization noise.

Chapter 4

PLL-Based Polar RF-PWM Transmitter[1]

4.1 Introduction

The demand for Machine-to-Machine communications (M2M) is expected to increase rapidly over the next decade, with proliferation of IoT applications [40]. Simplicity of implementation, design flexibility and energy efficiency are expected to be key design drivers for M2M SoC solutions.

In recent years, standards have been proposed for machine-type communications in LTE [41]. Switching PA topologies offer a promising alternative for such 3G and LTE systems, due to their inherently high efficiency. Switch-based PA implementations also allow for utilization of deep submicron CMOS technologies. This is an enabler for single-chip SoC implementations that integrate RF PAs along with digital baseband and application processors, which can reduce cost and size.

A fully integrated transmitter architecture from baseband-to-RF that employs (RF-PWM) with a Class-D output stage (Fig. 4.1a) is described be-

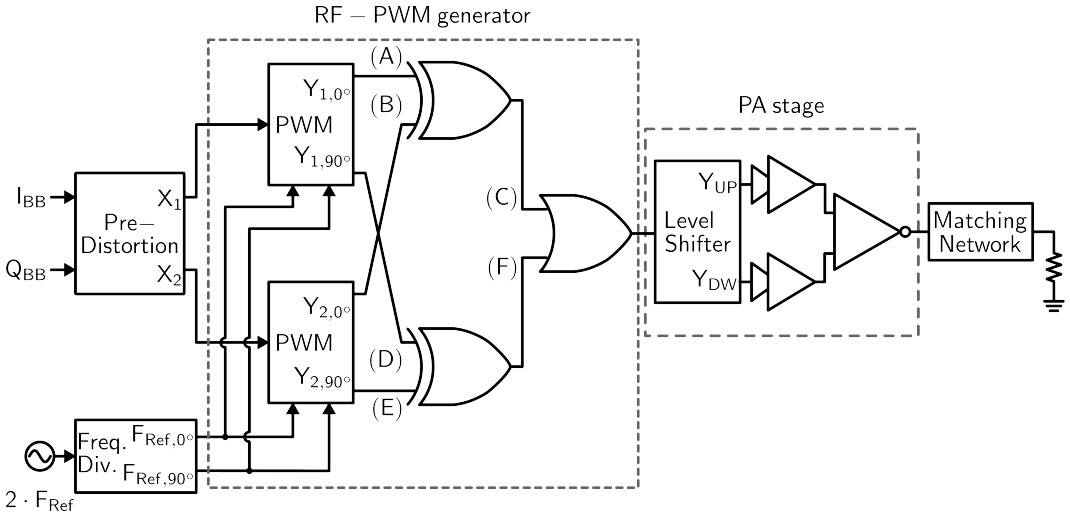
[1]Part of the material in this chapter is based on [1] which has been published in IEEE Radio Frequency Integrated Circuits Symposium, 2015. The author Hyejeong Song was responsible for the design, implementation and measurement of the transmitter IC described in the paper.

low. A PLL-based PWM generator [38] is used, since it allows for PWM generation without requiring high-speed linear ramp signals, or high-speed comparators. The RF-PWM transmitter proposed here employs two PLL-based pulse-width modulators, and uses a polar format which encodes amplitude information in the pulse duty cycle, and phase information in the pulse position. The use of polar signals requires higher bandwidth in the PLLs, compared to Cartesian inputs. However, since this application targets a relatively narrow bandwidth application (~1.4-MHz), a polar format is used, owing to its lower design complexity. PLL-based RF-PWM, as shown here, enables RF output generation without an upconverter or the requirement for complex digital signal processing for reducing out-of-band noise. Moreover, multiband operation can be achieved by changing the reference clock frequency of the pulse-width modulators. In conventional polar transmitter architectures a critical design challenge arises from the requirement to align the envelope and phase signals. The polar-based approach proposed here does not face this issue, since it uses input signals that include both the envelope and phase information simultaneously in the analog domain. By employing analog-domain comparison, it does not suffer from degradation caused by phase quantization.

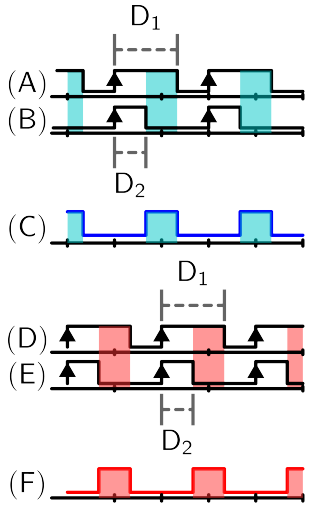
4.2 PLL-Based RF-PWM Transmitter

4.2.1 RF Pulse-Width-Modulation

RF-PWM encodes the envelope information $A_{BB}(t)$ and the phase information $\phi_{BB}(t)$ from the input signal into the pulse width and position

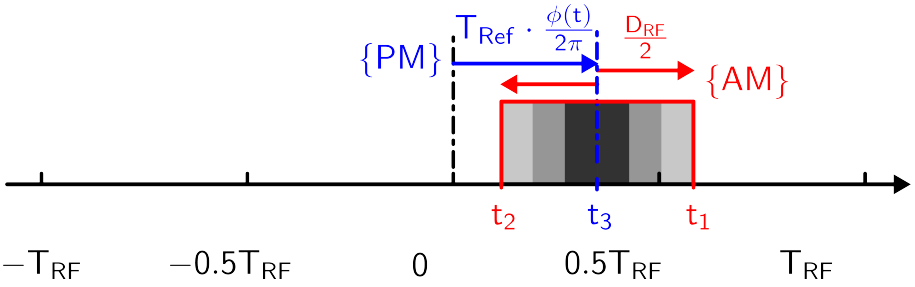


(a) The proposed RF-PWM transmitter

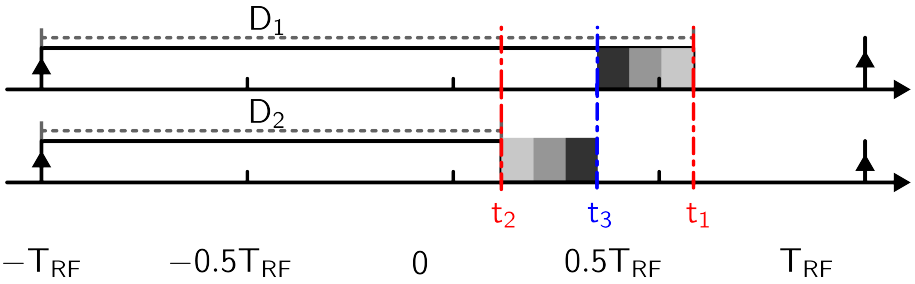


(b) Associated signals

Figure 4.1: The proposed RF-PWM transmitter and associated signals.



(a) RF-PWM



(b) Generation of RF-PWM using two edge-referred PWM pulses

Figure 4.2: RF-PWM generation

respectively (Fig. 4.2a) [3, 5]. The RF-PWM signal can be shown to be given by:

$$V_{out}(t) = 2 \cdot D_{RF}(t) + \sum_{n=1}^{\infty} \left\{ \frac{2V_{DD}}{n\pi} \cdot sin\left(n\pi D_{RF}(t)\right) \cdot cos\left(\frac{2n\pi}{T_{RF}}t + n\phi_{BB}(t)\right) \right\} \tag{4.1}$$

The duty cycle $D_{RF}(t)$ in the above equation is proportional to the time-varying amplitude. T_{RF} is the carrier period, and the RF carrier frequency is given by $f_{RF} = 1/T_{RF}$. By pre-distorting the signal amplitude using a sin^{-1} function, and using the resulting signal $A_{PD}(t)$ in Eq. 4.1, the RF output signal, $V_{out}(t)$, can be generated at the carrier frequency ($f_{RF} = 1/T_{RF}$) without an up-converter. The duty cycle of the pulse is limited to 50% in order to ensure monotonicity with respect to the the input signal.

4.2.2 PLL-Based RF-PWM Transmitter

A baseband pulse-width modulator has a linear relationship between the input signal (X_{IN}) and the duty cycle (D), which is given by

$$D = K \cdot X_{IN} \tag{4.2}$$

The pulse width is modulated relative to a fixed clock edge, either rising or falling. For this type of modulation, it can be shown that information around the harmonics of the PWM carrier signal cannot be used for direct transmission, as it has a strongly non-linear dependence on the input signal.

RF-PWM, on the other hand, can be made perfectly linear at carrier harmonics using sin^{-1} pre-distortion as noted above. In this work, two PLL-based baseband PWM generators are used to generate RF-PWM. The proposed approach uses the difference between two PWM pulses whose falling edges (t_1 and t_2) coincide with the rising edge (t_1) and the falling edge (t_2) of the RF-PWM signal in Fig. 4.2a. By controlling the duty cycle of both pulses individually, the RF-PWM generator is able to control the duty cycle and center position of the output pulses without complex processing at RF.

In Fig. 4.2a, the phase information of the modulation is set by the time instant t_3, which is the mid-point of the transmitted rectangular pulse. This time instant can vary from $-0.5T_{RF}$ to $+0.5T_{RF}$, which corresponds to a phase variation of $\pm\pi$. Amplitude modulation is encoded in the width of the pulse, which can vary from 0 to $0.5T_{RF}$, with a maximum duty cycle of 50%, within an RF period of T_{RF}. To accommodate phase information from $-\pi$ to π while allowing for the maximum duty cycle of 50%, the possible range of the rising and falling edges of RF-PWM extends from $-0.75T_{RF}$ to $0.75T_{RF}$, respectively. This implies that maximum pulse width of the baseband PWM signals needs to be larger than $1.75T_{RF}$. In this design the period of the PWM generator (T_{PWM}) is chosen to be $2T_{RF}$, which determines the maximum pulse width. The RF-PWM generator is consequently able to generate one pulse in a $2T_{RF}$ period. To increase the carrier frequency of the RF-PWM signal, quadrature RF-PWM signals, each with a period of $2T_{RF}$, are interleaved. From Eq. 4.2, the location of each falling edge (t_1 and t_2) is given by

$$t_1 = D_1 \cdot (2T_{RF}) = K \cdot X_{IN,1}(t) \cdot (2T_{RF})$$
$$t_2 = D_2 \cdot (2T_{RF}) = K \cdot X_{IN,2}(t) \cdot (2T_{RF}) \tag{4.3}$$

The RF-PWM generator is shown in Fig. 4.1a. In the pre-distortion block, the input signal is used to generate two signals, $X_{IN,1}(t)$ and $X_{IN,2}(t)$, which are used to drive the two pulse-width modulators. These signals are derived using Eq. 4.1- Eq. 4.3 and are given by

$$X_{IN,1}(t) = \frac{A_{PD}(t)}{4} + \frac{1}{2K} \cdot \frac{\phi_{BB}(t)}{2\pi}$$
$$X_{IN,2}(t) = -\frac{A_{PD}(t)}{4} + \frac{1}{2K} \cdot \frac{\phi_{BB}(t)}{2\pi} \tag{4.4}$$

$A_{PD}(t)$ above is the pre-distorted amplitude signal at baseband. $A_{PD}(t)$ is generated from $A_{BB}(t)$, which is the amplitude component in the polar representation of the baseband signal. The complete polar representation is derived from the Cartesian inputs, and in addition to the amplitude $A_{BB}(t)$, also includes the phase term $\phi_{BB}(t)$. $A_{PD}(t)$ is given by

$$A_{PD}(t) = \frac{1}{\pi K}.sin^{-1}\left\{\frac{A_{BB}(t)}{2V_{DD}/\pi}\right\}. \tag{4.5}$$

A PLL-based pulse-width modulator (Fig. 4.3)[37, 38] is employed because, as noted previously, it does not require a high-speed ramp signal and comparator which are key challenges to designing a high-speed pulse-width modulator. In a PLL-based pulse-width modulator, the local average of the output of the phase detector (PD) follows the input signal due to the negative feedback loop. The PWM signal is observed at the output of the PD. The

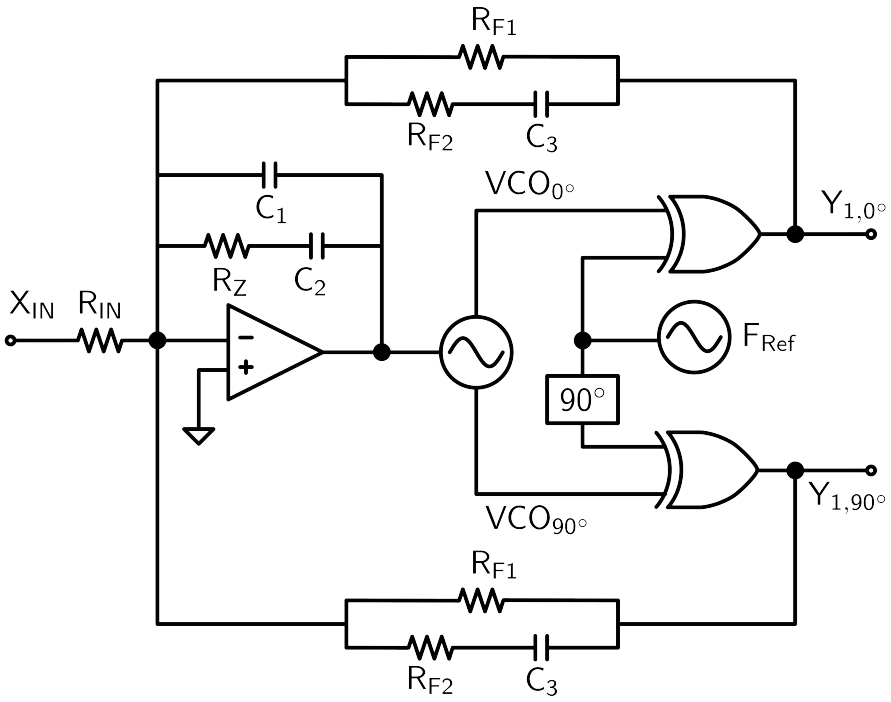


Figure 4.3: PLL-based PWM architecture

PD provides two pulses per reference-clock period (T_{Ref}) of the PLL, since it performs two comparisons within one period. As a result, the period (T_{PWM}) of the PWM signal is half of the clock period (T_{Ref}). The relationship between the input signal and the duty cycle of the PLL-based PWM modules is linear.

Baseband signals $X_{IN,1}(t)$ and $X_{IN,2}(t)$ are applied to independent PLL-based pulse-width modulators, each with its own quadrature VCO. Within each PLL, the phases of the quadrature VCO outputs are compared to quadrature reference signals. The reference clocks are generated from a single external clock source, by applying it to a divide-by-2 frequency divider. Each of the PLL-PWM generators thus provides two PWM outputs that are in quadrature. These are indicated as $Y_{1,0^\circ}$ and $Y_{1,90^\circ}$, and $Y_{2,0^\circ}$ and $Y_{2,90^\circ}$ in Fig. 4.1a. Quadrature RF-PWM outputs with a period of T_{PWM} are achieved by combining $Y_{1,0^\circ}$ and $Y_{2,0^\circ}$, and $Y_{1,90^\circ}$ and $Y_{2,90^\circ}$ by using an EX-OR phase detector. These quadrature outputs are then combined using an OR operation.

The reference clock period ($T_{Ref} = 2T_{PWM} = 4T_{RF}$) for the PWM provides additional phase margin that helps to alleviate PLL bandwidth requirement. The phase information is usually wrapped in a range from $-\pi$ to π, which causes a phase discontinuity, if the original modulation includes phase steps from $\pm\pi$ to $\mp\pi$[2]. The RF-PWM generator using interleaving provides a wider phase margin from -1.5π to 1.5π, which can be used to correct the

[2]A phase jump of $\pm\pi$ in the RF carrier corresponds to a pulse time variation of $\pm T_{RF}/2$ or equivalently, $\pm T_{REF}/8$. Since the linear range of a PLL-PWM block is $T_{REF}/2$ (Fig. 3.4d), this phase jump can be accommodated by the PLL-PWM block.

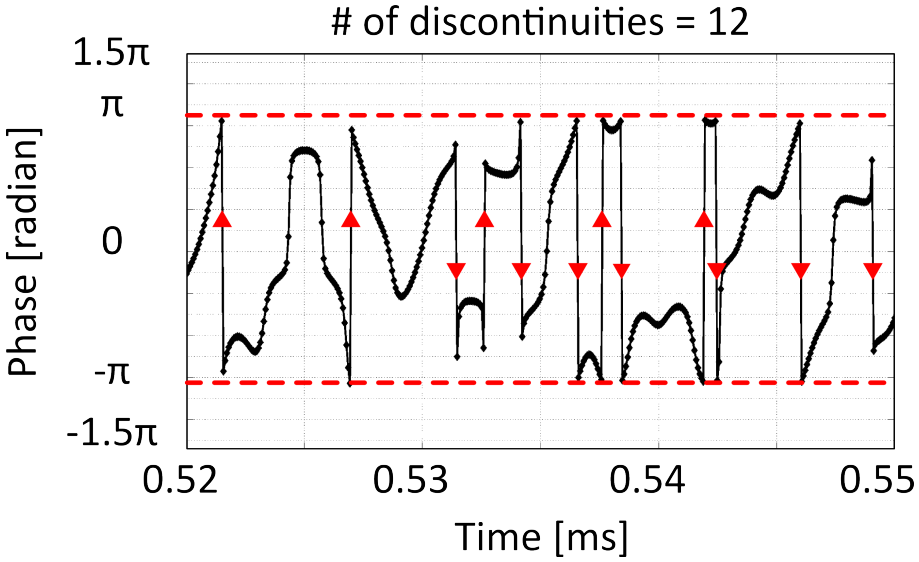
radian phase angles by adding multiples of $\pm 2\pi$ when absolute jumps between consecutive phase steps are greater than or equal to the jump tolerance allowed by the PLL-bandwidth. Phase discontinuities can only occur now for phase steps from $\pm 1.5\pi$ to $\mp 1.5\pi$, whose probability of occurrence is lower than that of a phase step from $\pm\pi$ to $\mp\pi$. As shown in Fig. 4.4, the total phase jump rate in the LTE signal is decreased by up to 58%.

4.3 Analysis of the Proposed Architecture

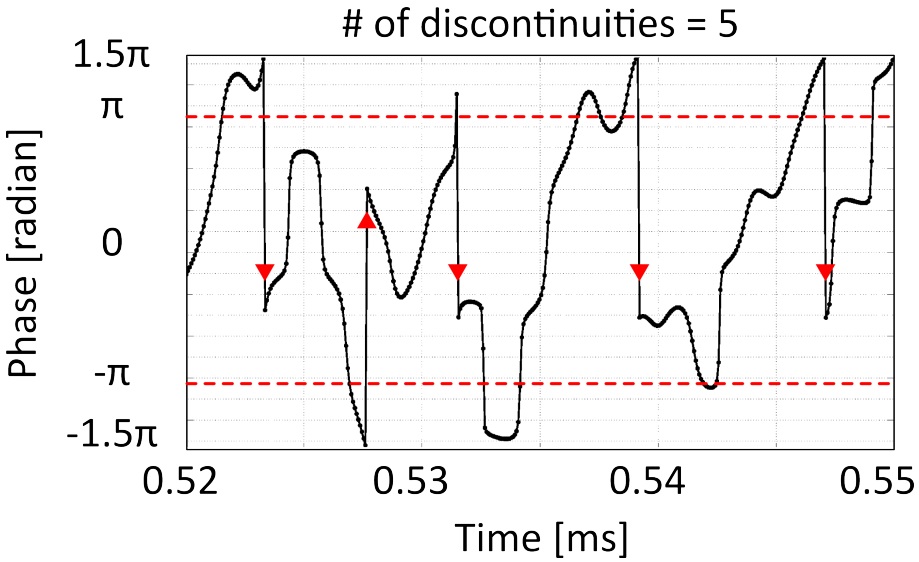
This section presents an analysis of noise in the architecture. The derivation employs linearized models for the circuit blocks shown in Fig. 4.1a, including the EX-OR phase detectors. The models are used to calculate the phase noise of the PLL-based pulse-width modulators, while considering major noise sources. A noise model for the RF-PWM output is presented.

4.3.1 Linearized Model of EX-OR Phase Detector

The EX-OR phase detectors generate signals representing the difference in phase between the VCO and the reference. The output of the phase detectors is fed to the RF-PWM generator as well as to the loop filter for feedback to the PLL-based pulse-width modulator. Phase detection is a memoryless operation. As such its impact on the behavior of the loop can be modeled by a constant gain [39, 38]. The loop-dynamics of the PLL-based pulse-width modulators are primarily governed by the baseband frequency response. On the other hand, the simple model is not adequate for analysis of the RF-PWM



(a) Original phase



(b) Corrected phase

Figure 4.4: Phase trajectory with LTE signal

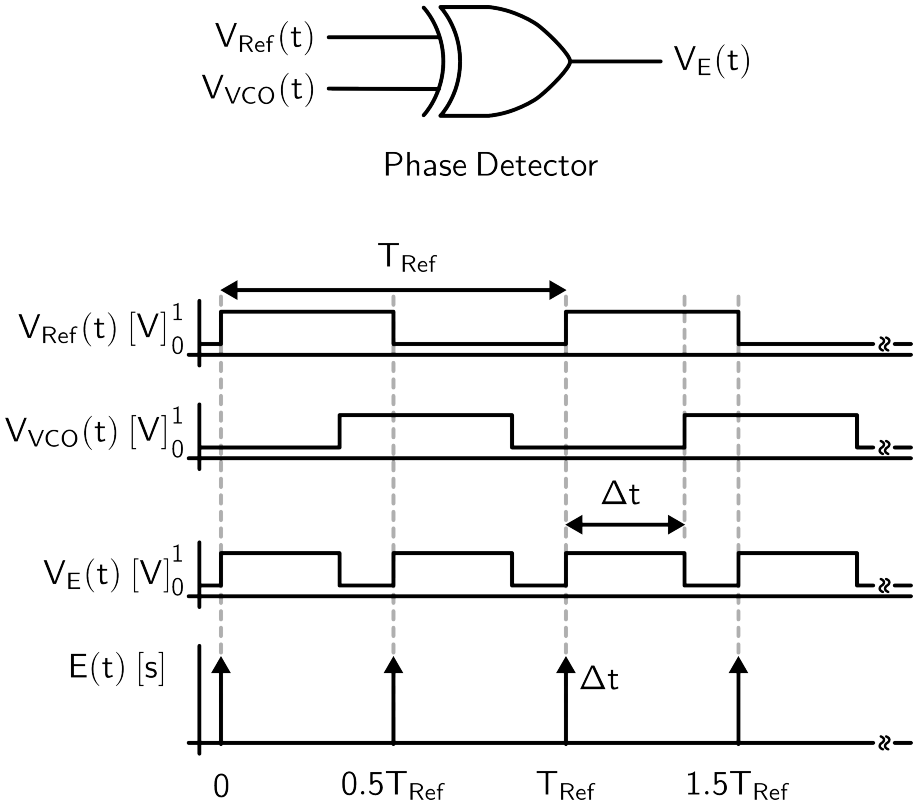


Figure 4.5: EX-OR phase detector and associated signals

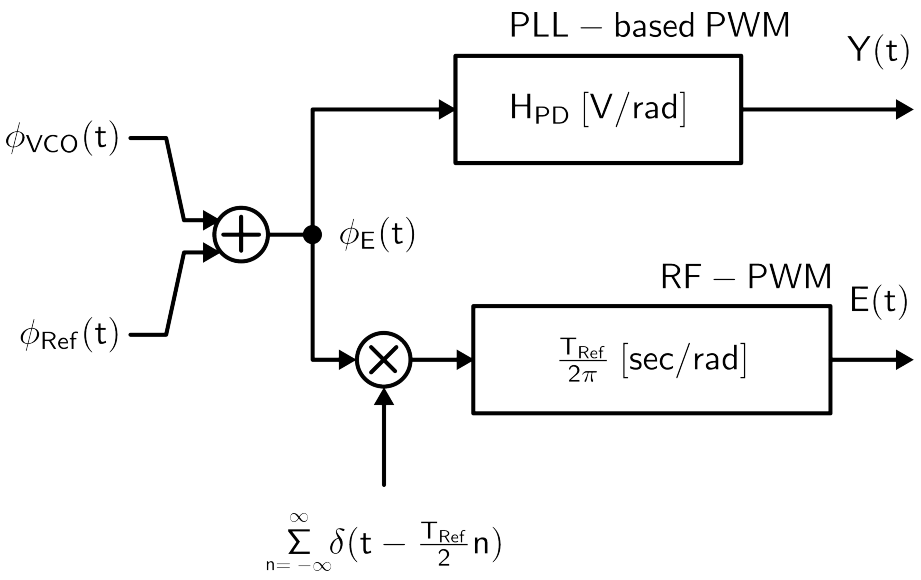


Figure 4.6: Linear model of EX-OR phase detector.

generator, which employs baseband and higher harmonics. For frequency domain analysis of RF-PWM, the output signals of the EX-OR phase detector are represented by impulse sequences, with the input phase difference as a parameter.

Fig. 4.5 shows the EX-OR phase detector and signals which is associated with the operation of the EX-OR phase detector. The output of the detector $V_E(t)$ consists of pulse sequences whose width (Δt) is encoded by the relative phase difference between the VCO output ($V_{VCO}(t)$) and the reference signal ($V_{Ref}(t)$) at the rising and falling edges respectively. The actual pulse-width modulated output of the detector ($V_E(t)$) can be formulated as an infinite sum of various harmonics. RF-PWM, however, utilizes the pulse width information rather than the voltage transients, which makes it possible

to simplify the output ($V_E(t)$) as a sequence of impulses weighted by the time-varying pulse width (Δt(t)) instead of a modulated pulse [39]. The impulse sequence ($E(t)$) can be defined as

$$E(t) = \Delta t(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - \frac{T_{Ref}}{2}n). \tag{4.6}$$

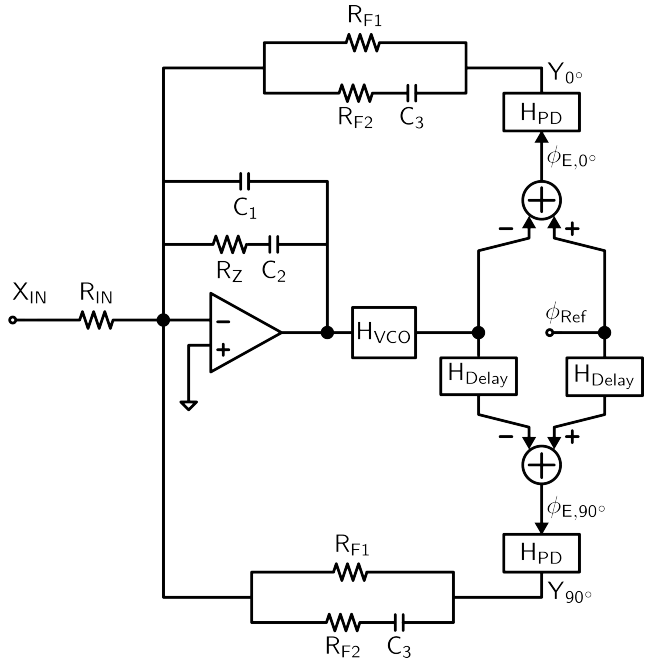
Since the bandwidth of the input signal is about two orders of magnitude lower than the reference, VCO frequency variations are not significant in a time window that is short compared to the inverse of the signal bandwidth, in the locked condition. Therefore, the relationship of Δt to the phase difference can be approximated as

$$\Delta t(t) \approx \frac{T_{Ref}}{2\pi}\phi_E(t) \tag{4.7}$$

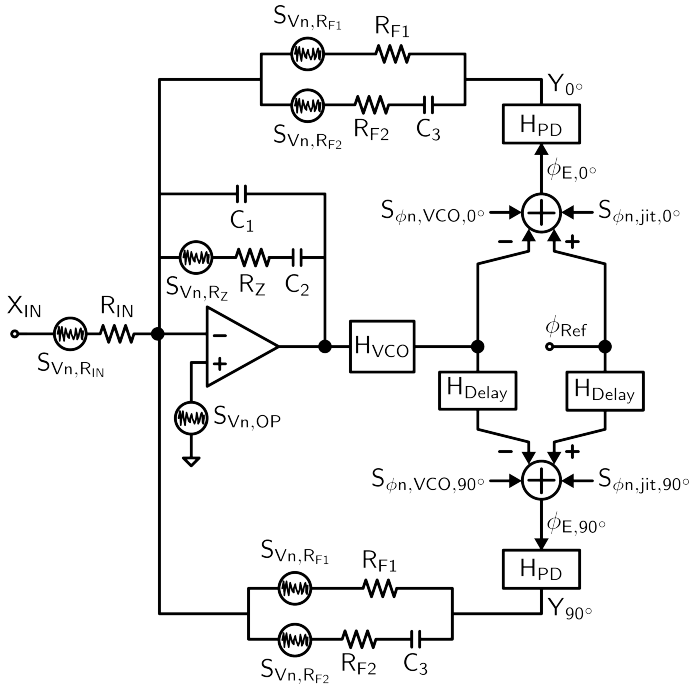
where $\phi_E(t)$ denotes the phase difference between the VCO output and the reference signal. Combining Eq. 4.6 and Eq. 4.7, the pulse width of pulse-width modulator can be modeled as

$$E(t) = \frac{T_{Ref}}{2\pi} \cdot \phi_E(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - n\frac{T_{Ref}}{2}). \tag{4.8}$$

Fig. 4.6 illustrates the resulting model of the phase detectors. The baseband components ($Y(t)$), and pulse width sequences ($E(t)$) are utilized for analysis of the PLL-based pulse-width modulator, and the RF-PWM generator respectively.



(a) Linear model of PLL-based PWM



(b) Linear model with noise sources

Figure 4.7: Linear model of PLL-based PWM

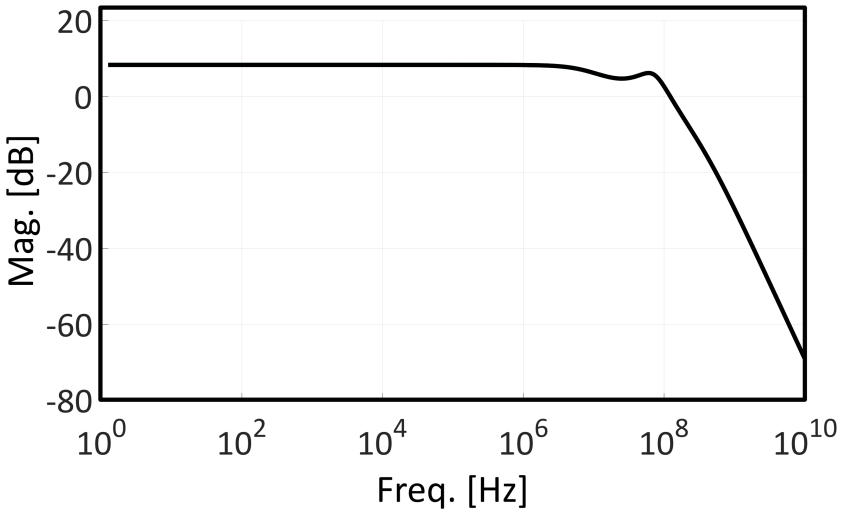


Figure 4.8: Magnitude response of $\phi_{E,0^\circ}(j\omega)/X_{In}(j\omega)$

4.3.2 Linear Model of the PLL-Based Pulse-Width Modulator

The linear model of the PLL-based pulse-width modulator is shown in Fig. 4.7a. The loop shown in Fig. 4.7a is practically a type-II Phase-Lock Loop (PLL), although it includes an additional loop to generate a 90° phase-shifted output simultaneously. The quadrature VCO (H_{VCO}) is modeled as an ideal integrator with a gain (K_{VCO}). Two delay blocks shown as (H_{Delay}) are connected to the reference and the VCO respectively and model the quadrature phase-shifted VCO and reference signals. The phase detector provides a gain (H_{PD}) of $-\frac{V_{DD}}{\pi}$, assuming that the PD output switches between 0 and V_{DD}. The frequency response of the operational amplifier is given by $A_{OP}(j\omega)$. Using the above notation, the loop gain, $A_{OL}(j\omega)$, and the resulting transfer function, $\frac{\phi_{E,0^\circ}(j\omega)}{X_{IN}(j\omega)}$, can be shown to be given by:

$$A_{OL}(j\omega) = \frac{-A_{OP}(j\omega)(1+H_{Delay}(j\omega))Z_{LF}(j\omega)H_{VCO}(j\omega)H_{PD}}{(A_{OP}(j\omega)+1)Z_F(j\omega)+Z_{LF}(j\Omega)\{Z_F(j\omega)/R_{IN}+2\}} \quad (4.9)$$

$$(4.10)$$

$$\frac{\phi_{E,0^\circ}(j\omega)}{X_{IN}(j\omega)} = \frac{A_{OL}(j\omega)}{1-A_{OL}(j\omega)} \cdot \frac{Z_F(j\omega)/R_{IN}}{H_{PD}\{1+H_{Delay}(j\omega)\}} \quad (4.11)$$

where $Z_{LF}(j\omega)$ is the transfer function of the input low-pass filter and is given by $Z_{LF}(j\omega) = 1/(j\omega C_1) \parallel (R_Z + 1/(j\omega C_2)$; $Z_F(j\omega)$ is the feedback impedance, where $Z_F(j\omega) = R_{F1} \parallel (R_{F2} + 1/(j\omega C_3)$; and $H_{Delay}(j\omega)$ models the frequency response of the quadrature phase shift in the VCO and the reference, where $H_{Delay}(j\omega) = e^{-j\omega T_{ref}/2}$.

From Eq. 4.9, $A_{OL}(j\omega)$ can be seen to be given by $-\frac{4\pi}{3} \cdot A_{OP}(j\omega) \cdot K_{VCO} \cdot H_{PD}/j\omega$ for low-frequencies since $Z_{LF}(j\omega)$ has a large impedance($\approx \frac{1}{0}$). $Z_F(j\omega)$ and $H_{Delay}(j\omega)$ are given by a constant resistance (R_{F1}) and a constant value 1, respectively, at low-frequencies. The magnitude response of $\phi_{E,0^\circ}(j\omega)/X_{IN}(j\omega)$ is shown in Fig. 3.7. The magnitude of $\phi_{E,0^\circ}(j\omega)/X_{IN}(j\omega)$, from Eq. 4.11, has a constant gain, π/V_{DD}, within the signal bandwidth of the input X_{IN}. Using this result in Eq. 4.7, the coefficient K that relates the duty-cycle D to the input X_{IN} in Eq. 4.2 can be shown to be

$$K = \frac{D}{X_{IN}} = \frac{T_{Ref}}{2\pi} \cdot \frac{2}{T_{Ref}} \cdot \frac{\phi_{E,0^\circ}}{X_{IN}} = \frac{1}{V_{DD}}. \quad (4.12)$$

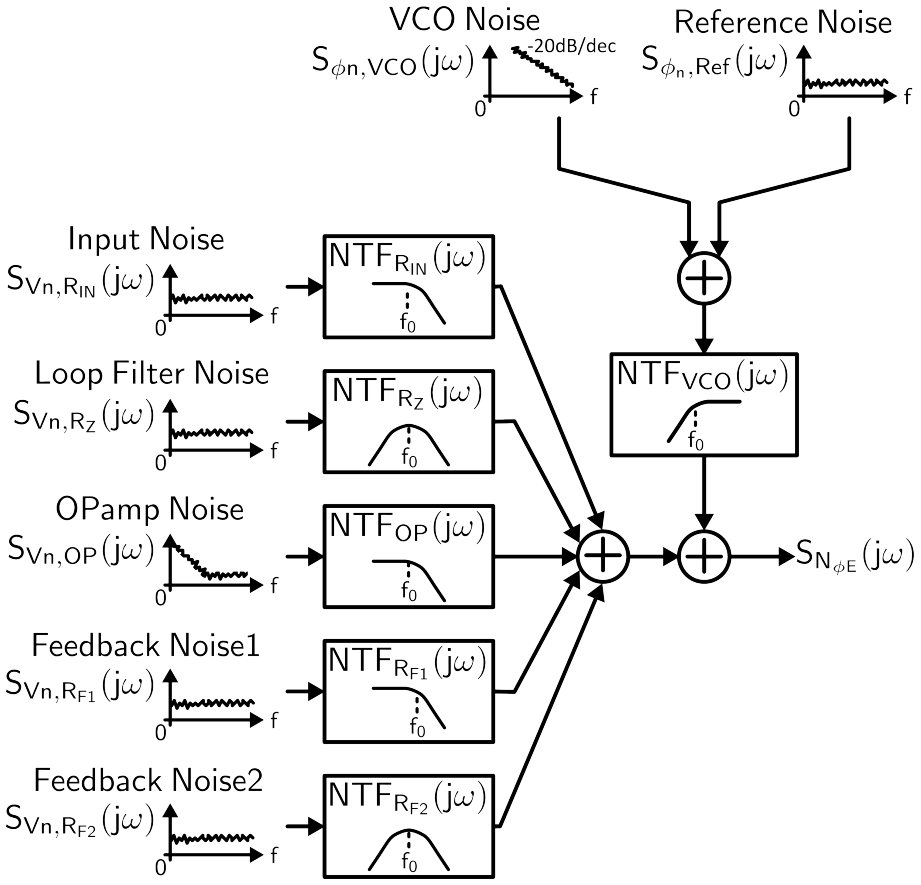


Figure 4.9: PLL noise

4.3.3 Noise Analysis of PLL-Based Pulse-Width Modulator

By using the linear noise model shown in Fig. 4.7b, the noise transfer function (NTF) from various noise sources to the phase error ($\phi_{E,0^\circ}$) can be shown to be

$$
\begin{aligned}
NTF_{VCO}(j\omega) &= \{1 + G(j\omega)\} \\
NTF_{RIN}(j\omega) &= G(j\omega) \cdot \frac{Z_F(j\omega)/R_{IN}}{H_{PD} \cdot \{1 + H_{Delay}(j\omega)\}} \\
NTF_{OPAMP}(j\omega) &= -G(j\omega) \cdot \frac{1 + Z_{LF}(j\omega) \cdot \{Z_F(j\omega)/R_{IN} + 2\}}{Z_{LF}(j\omega) \cdot H_{PD} \cdot \{1 + H_{Delay}(j\omega)\}} \\
NTF_{RF1}(j\omega) &= G(j\omega) \cdot \frac{Z_F(j\omega)}{R_{RF} \cdot H_{PD} \cdot \{1 + H_{Delay}(j\omega)\}} \\
NTF_{RF2}(j\omega) &= G(j\omega) \cdot \frac{Z_F(j\omega) \cdot \{j\omega C_3 + R_F\}}{j\omega C_3 \cdot R_F \cdot H_{PD} \cdot \{1 + H_{Delay}(j\omega)\}} \\
NTF_{Rz}(j\omega) &= G(j\omega) \cdot \frac{Z_F(j\omega) \cdot \{j\omega C_2 + R_Z\}}{j\omega C_2 \cdot R_Z \cdot H_{PD} \cdot \{1 + H_{Delay}(j\omega)\}}
\end{aligned}
\tag{4.13}
$$

where $G(j\omega) = A_{OL}(j\omega)/\{1 - A_{OL}(j\omega)\}$. Fig. 4.9 summarizes the frequency response of the various NTFs and noise sources for the spectral noise power ($S_{N_{\phi_E}}$) of the total phase error. Both the VCO noise and the reference noise are high-pass filtered by the loop, which results in suppression of these noise sources over a wide frequency range, within the system bandwidth. These noise sources, however, still have a dominant effect on the out-of-band noise, which sets a design constraint on the distant noise of the VCO and the reference.

The noise sources within the analog filter are low-pass filtered, while the noise of the R-C-C low-pass filter is band-pass filtered by the loop. These noise sources impact the spectral noise power ($S_{N_{\phi_E}}$) arising from the in-band phase error.

4.3.4 Linear Model of the RF-PWM Generator

Fig. 4.10 illustrates the linear model of the RF-PWM generators. The RF-PWM generator consists of two EX-OR and one OR gates where the envelop information (A_{BB}) and phase information (ϕ_{BB}) are encoded in the duty cycle (D_{RF}) and position of the pulse, respectively. The EX-OR function detects the difference and the mid-point of the falling edges of the input PWM signals, while the OR function combines the two PWM signals to realize interleaving. Employing impulse approximation, these operations can be simply modeled as an addition and subtraction of impulses, which makes it possible to change the order of the EX-OR and OR functions by applying the commutative property.

The pulse width of PWM signal can be modeled as impulse sequences $E_{m,n}(t)$ where the subscript m denotes the index of the PLL-based PWM generator and can assume values of 1 or 2. The subscript n signifies output signals with phase of 0°and 90°. The frequency response of pulse width sequences ($E_{m,n}(t)$) that is sampled with a period $T_{Ref}/2$ can be found by

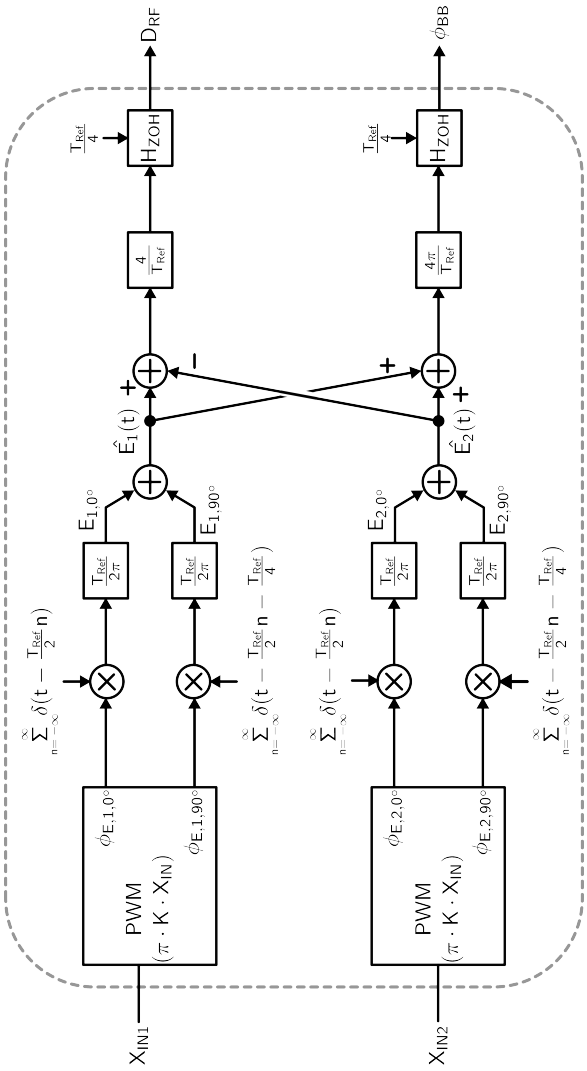


Figure 4.10: Linear model for the proposed RF-PWM architecture

employing Fourier Transform of Eq. 4.8, which leads to

$$E_{m,n}(j\omega) = \frac{2}{T_{Ref}} \sum_{k=-\infty}^{\infty} \frac{T_{Ref}}{2} \cdot K \cdot X_m(j\omega - \frac{4\pi n}{T_{Ref}}), \qquad \begin{cases} m & = 1 \ or \ 2 \\ n & = 0^\circ \ or \ 90^\circ \end{cases}. \tag{4.14}$$

In the time domain, $E_{m,90^\circ}(t)$ is a $T_{Ref}/4$ time-shifted version of $E_{m,0^\circ}(t)$. Representing this time-delay by a phase shift, the output of OR gate can be formulated as:

$$\begin{aligned} \hat{E_m}(j\omega) &= \frac{2}{T_{Ref}} \sum_{n=-\infty}^{\infty} (1 + e^{-j\omega \frac{T_{Ref}}{4}}) \cdot \frac{T_{Ref}}{2} \cdot K \cdot X_m(j\omega - \frac{4\pi n}{T_{Ref}}) \\ &\approx \frac{4}{T_{Ref}} \sum_{n=-\infty}^{\infty} \frac{T_{Ref}}{2} \cdot K \cdot X_m(j\omega - \frac{8\pi n}{T_{Ref}}) \end{aligned} \tag{4.15}$$

Eq. 4.15 indicates that the output of the OR function can be interpreted as a 2x signal up-sampler. The EX-OR function encodes the duty cycle information and the phase information in a pulse, which can be separately modeled as an addition and subtraction respectively, with corresponding constant gains.

We employ the impulse approximation to analyze the functionality of the RF-PWM generator which encodes the information to the pulse width with the fixed amplitude. To analyze the noise of the RF-PWM architecture, we need to convert signals from the discrete time domain to the analog domain. By applying a zero-order-hold reconstruction filter with $T_{REF}/4$ sampling time, we can transfer the analysis domain from discrete-time to analog. As a result, we can remove the impulse approximation for signal analysis. Thus the duty

cycle and the phase offset of RF-PWM can be formulated as

$$\begin{aligned} D_{RF}(j\omega) &= 2K \cdot (X_1(j\omega) - X_2(j\omega)) \\ \phi_{BB}(j\omega) &= 2\pi K \cdot (X_1(j\omega) + X_2(j\omega)). \end{aligned} \tag{4.16}$$

4.3.5 Noise Analysis of RF-PWM generator

In contrast to Eq. 4.15, the noise transfer function from the phase detector to the output of the OR logic can not be represented by a 2x up-sampler, since the two noise sources are independent and thus are not related by a time-shift. Instead of an up-sampler, the two noises are independently added in the OR logic circuit. As a result, the individual noise sources are sampled and reconstructed at $2/T_{Ref}$ and $4/T_{Ref}$ frequencies respectively, which indicates that we need to consider additional constant sampling/reconstruction gains of 0.5 for each phase noise term. By using the transfer function provided from Fig. 4.10 and total phase error spectral noise power ($S_{N_{\phi_E}}$) provided from Fig. 4.9, we can derive the duty cycle spectral noise power ($S_{D_N}(j\omega)$) and phase spectral noise power ($S_{\phi_N}(j\omega)$),

$$S_{D_N}(j\omega) = \frac{1}{\pi^2}\left\{S_{N_{\phi_{E,1,0^\circ}}}(j\omega) + S_{N_{\phi_{E,2,90^\circ}}}(j\omega) + S_{N_{\phi_{E,2,0^\circ}}}(j\omega) + S_{N_{\phi_{E,2,90^\circ}}}(j\omega)\right\}$$

$$S_{\phi_N}(j\omega) = \left\{S_{N_{\phi_{E,1,0^\circ}}}(j\omega) + S_{N_{\phi_{E,2,90^\circ}}}(j\omega) + S_{N_{\phi_{E,2,0^\circ}}}(j\omega) + S_{N_{\phi_{E,2,90^\circ}}}(j\omega)\right\}. \tag{4.17}$$

Based on Eq. 4.1, the RF-PWM with noise at the RF carrier frequency

can be derived as

$$V_{out,RF}(t)+N(t) = \frac{2V_{DD}}{\pi} sin(\pi(D_{RF}(t)+D_N(t)))cos(2\pi f_{RF}t+\phi_{BB}(t)+\phi_N(t)) \tag{4.18}$$

By employing a Taylor series expansion for a given $D_{RF}(t)$ and $\phi_{BB}(t)$, while assuming $D_N(t)$ to be small,we have,

$$\begin{aligned} V_{out,RF}(t) + N(t) = \approx & \frac{2V_{DD}}{\pi} sin(\pi D_{RF}(t))cos(2\pi f_{RF}t + \phi_{BB}(t)) \\ & + \frac{2V_{DD}}{\pi}\pi D_N(t)cos(\pi D_{RF}(t))cos(2\pi f_{RF}t + \phi_{BB}(t)) \\ & - \frac{2V_{DD}}{\pi}\phi_N(t)sin(\pi D_{RF}(t))sin(2\pi f_{RF}t + \phi_{BB}(t)) \end{aligned} \tag{4.19}$$

Combining Eq. 4.17 and Eq. 4.19, we can relate the total spectral noise power $S_{N(t)}(j\omega)$to the RF-PWM phase error noise by

$$S_{N(t)}(j\omega) = \frac{1}{2} \cdot (\frac{2V_{DD}}{\pi})^2 \cdot 4S_{N_{\phi_E}}(j\omega) \tag{4.20}$$

where we assume that the individual phase error spectral noise power ($S_{N_{\phi_E}}(j\omega)$) introduced by the EX-OR phase detectors is the same. The RF-PWM noise can be modeled as a total sum of phase noise of each PLL-based PWMs. As a result, the in-band and out-of-band noise are strongly dependent on the noise of the analog filter and the VCO within the PLL-based pulse-width modulator respectively. In following section, we will discuss how to take this noise into consideration in the circuit implementation.

4.4 Circuit Implementation

4.4.1 PLL-Based Pulse-Width Modulator

The pulse width modulator of [38] targets power line communication, where the bandwidth and carrier frequency of the pulse-width modulator is lower than the wireless RF transmitter described here. The wider bandwidth introduces additional design challenges, as described below.

The key design considerations in this work include the linearity of the PLL-based PWM system and noise minimization. Since the design uses two PLL-based pulse-width modulators, it is also critical to minimize mutual coupling. For this purpose, the power supply in the two PLL-based PWMs is separated. Further the physical spacing between the pulse-width modulator is maximized in layout, to the limit set by the size of the IC.

4.4.1.1 Loop Design

The gain and the phase margin of the loop are directly related to noise, linearity, and system bandwidth. Such margins can be controlled by choosing the ratio (C_1/C_2) of the loop capacitance, the ratio ($R_{IN}/(R_{F1} \parallel R_{F2})$) of the resistance in the active filter and the gain (K_{VCO}) of VCO. The loop stability with a time-varying input signal is important to consider. The maximum allowable rate-of-change of the input signal can be determined by the ratio of resistor in input and feedback loop, the gain of VCO, and the range of VCO's control voltage, and it can be shown to be [38]

$$max(\frac{dX_{IN}}{dt}) = 4K_{VCO}V_{DD}\frac{R_{IN}}{Z_F} \cdot max(V_{VCO}).$$

The proposed architecture has two loops with a relative 90° degree phase shift and split feedback, which provides smaller changes in V_{VCO} compared to a single loop feedback for the same input signal level. As a result, it provides better linearity and stability.

The proposed RF-PWM transmitter requires that the two PWM generators have identical performance, in order to minimize the mismatch and the distortion. The split dual-feedback can be helpful for minimizing the mismatch between the two VCOs by reducing the input range of the VCO control voltage.

In this work, the implemented loop provides 45° degree phase margin with an unity gain bandwidth of 100-MHz, in order to ensure sufficiently fast settling, and guarantee good stability over device process corners.

4.4.1.2 Clock Duty Cycle

The duty cycle of the clock signal in PLL-based PWM determines the dynamic range of the output voltage. The duty cycle of the clock signal, which provides the maximum dynamic range, is 50% [38]. To guarantee 50% duty cycle for both the clock signal and the VCO output signal, a frequency divider and differential architecture are used. In order to ensure a square pulse shape, a CMOS buffer chain with cross coupled inverters is employed [42].

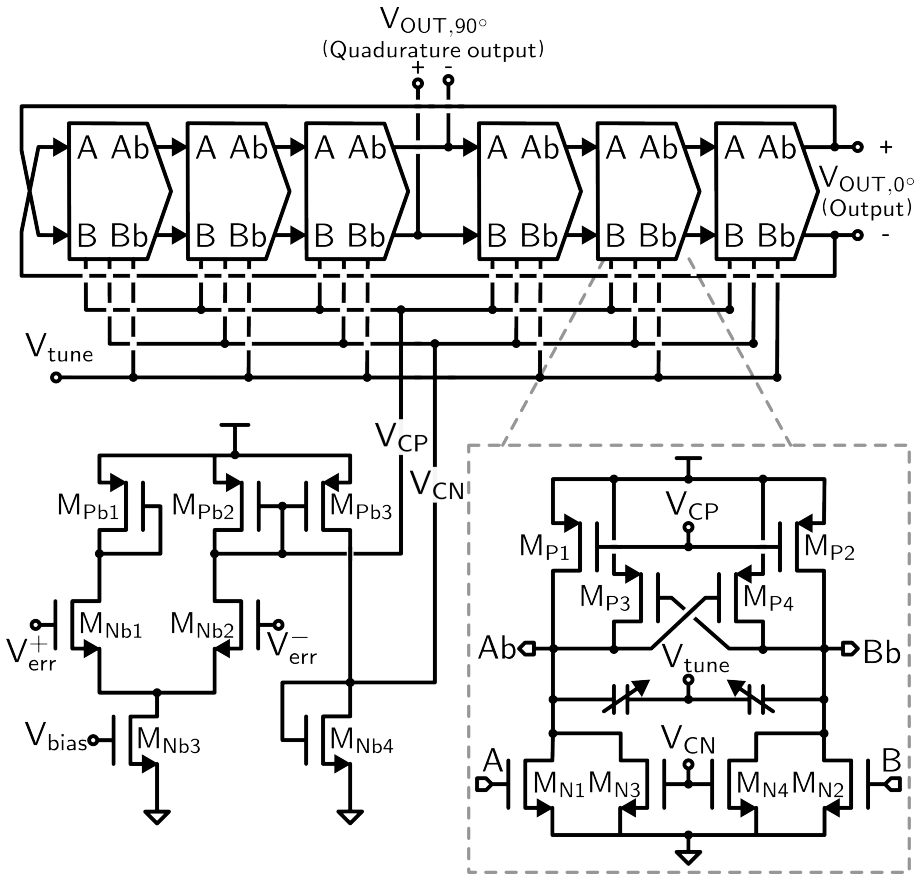


Figure 4.11: Differential quadrature VCO

4.4.1.3 VCO

A six-stage VCO (Fig. 4.11) is used in the design. Each delay cell in the VCO provides rail-to-rail swing. It achieves a well-controlled 50% duty cycle through the use of a differential design. The digitally intensive design allows for wideband PWM operation.

The gate nodes of NMOS switches (M_{n1},M_{n2}) are the inputs of a delay cell. The switches are connected to the output nodes of the cell. The delay cell also consists of cross-coupled PMOS transistors (M_{p3} and M_{p4}) for fast switching. Coarse tuning is achieved by varying the voltage (V_{tune}) of the varactors which are connected across the output nodes. For a fine control of the oscillation frequency, auxiliary PMOS transistors (M_{p1}, M_{p2}) and NMOS transistors (M_{n3}, M_{n4}) are employed. The design uses a 1.2-V power supply. The VCO provides in-phase and quadrature outputs. The simulated gain of the VCO is 350-MHz/V. The intermodulation components which are observed in Eq. 3.1 are reduced through the use of a differential topology, which helps to mitigate even order harmonics.

4.4.1.4 Operational Amplifier

The operational amplifier that is employed in the low pass filter is shown in Fig. 4.12. The design employs a fully differential two-stage topology to reduce even-order distortion. PMOS devices are used in the input stage for better isolation from substrate noise and lower flicker noise. The device channel length is optimized to improve noise performance, while providing adequate

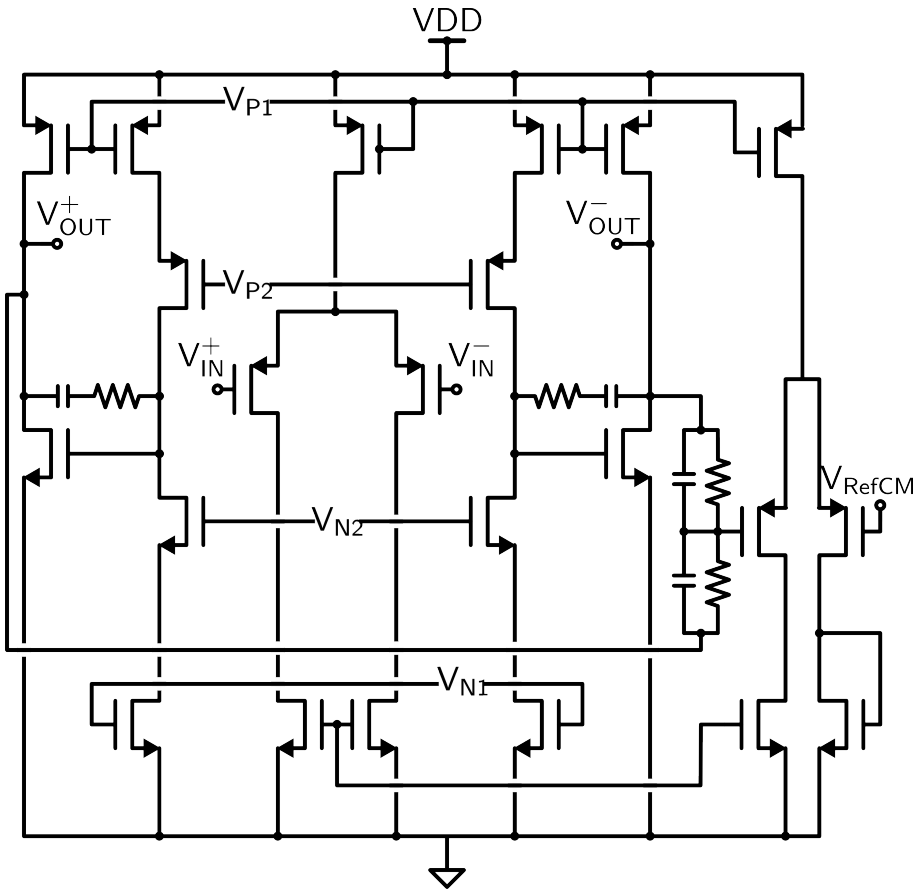


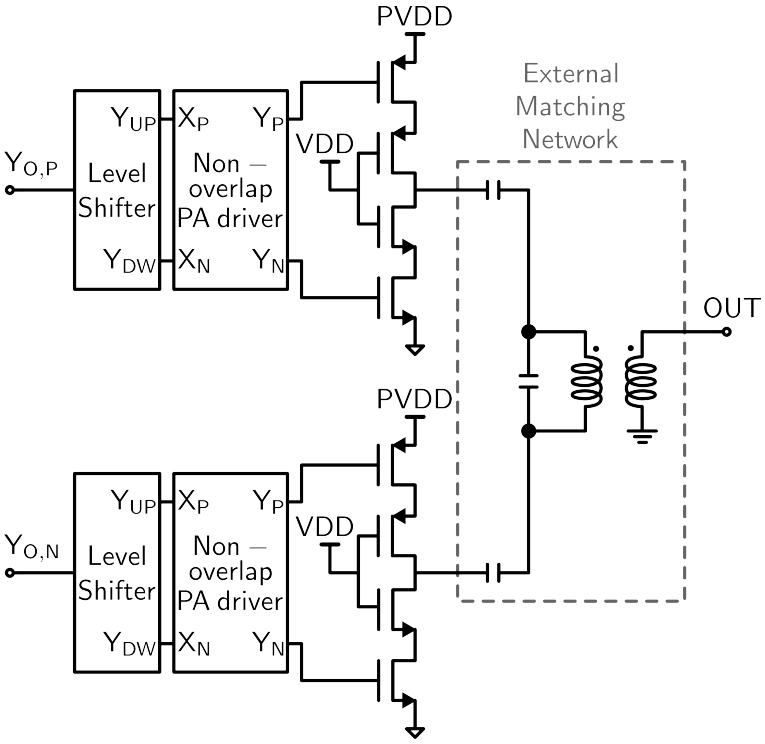
Figure 4.12: Operational amplifier

frequency response. The OPAMP open-loop gain is 56 dB. The gain of the low pass filter is one of critical design factors because it suppresses the impact of K_{VCO} non-linearity. The total current consumption is approximately 10 mA in the OPAMP.

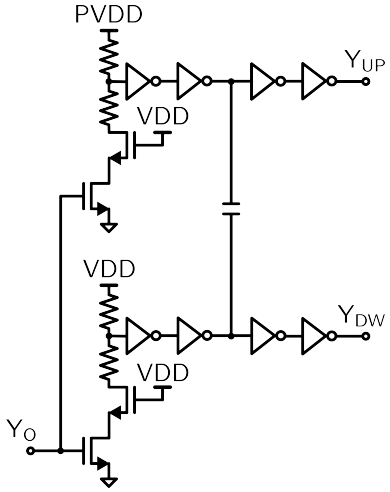
4.4.2 Power Amplifier and Driver

The output stage (Fig. 4.13) includes level shifters, PA drivers, Class-D PAs and an external matching network. A stacked inverter is used in the PA. This design requires a level shifter to interface the RF-PWM signal to the cascode output stage. The level shifter consists of a simple cascode to allow for high speed operation (Fig. 4.13b). For balancing the rise and fall times of the pulses, a coupling capacitor is used between the branches of the cascode.

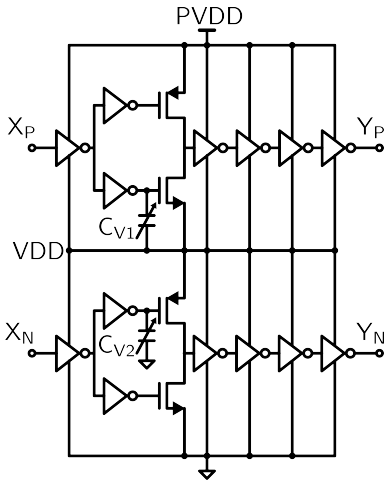
In order to minimize shoot-through currents, separate PA drivers are employed for the PMOS and NMOS devices within the output stage. These convert the RF-PWM signal into non-overlapping control signals. However these signals can have different rise and fall times, which can cause non-linearity in the output stage. Controlling the capacitance (C_{V1} and C_{V2}) in each path of the PA driver (Fig. 4.13c), allows for making the rise and fall times equal, and also allows for simultaneously optimizing efficiency and linearity. The entire signal path is differential, which helps to mitigate the impact of bond-wire parasitics and common-mode noise.



(a) Output stage

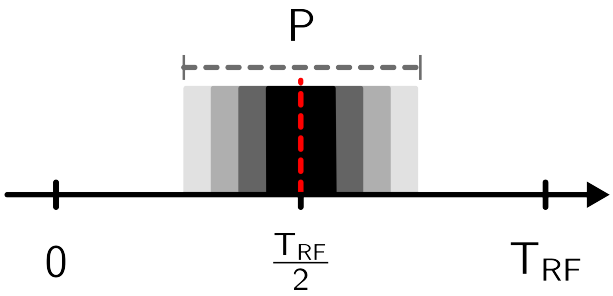


(b) Level shifter

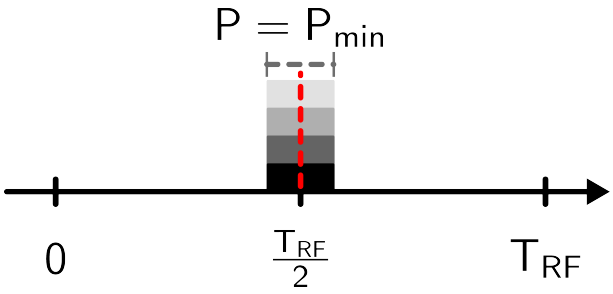


(c) PA driver

Figure 4.13: Circuits for the output stage

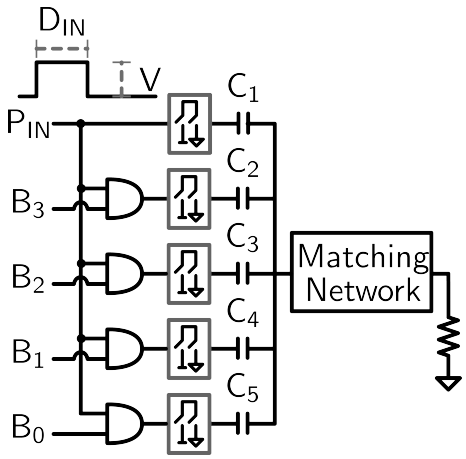


(a) Pulse modulation for $P > P_{MIN}$

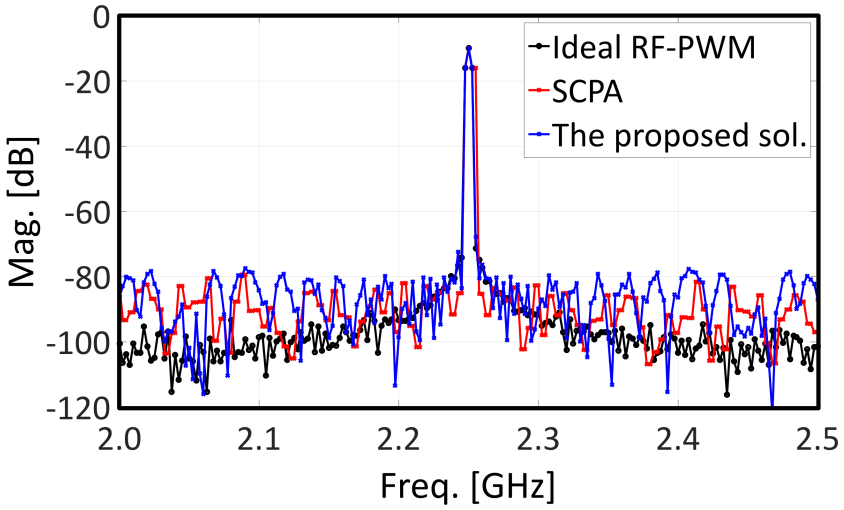


(b) Supply modulation for $P < P_{MIN}$

Figure 4.14: Proposed solution to address the narrow-pulse limitation



(a) Diagram of the proposed hybrid solution



(b) Output signal FFT (simulation results)

Figure 4.15: Proposed narrow pulse solution and simulation results

4.5 Avoiding the Narrow Pulse-Width Limitation

Since RF-PWM encodes the information to the pulse width of the signal, the dynamic range is determined by the pulse width range which is available to handle in the system. In practical CMOS technologies, device parasitic capacitance limits the minimum pulse width that can be generated in the class-D stage. This sets a limit on the dynamic range, since below a certain minimum amplitude, the output duty-cycle does not follow the input duty-cycle linearly.

To solve the narrow pulse problem, an approach based on a switched capacitor power amplifier (SCPA) [23] can be employed in order to control the amplitude of output signal in addition to PWM. For narrow pulse widths, the amplitude of the output can be varied while keeping the pulse width fixed (Fig. 4.14b). By adopting SCPAs, the amplitude of the RF-PWM output can be controlled using digital control bits.

The proposed concept is shown in Fig. 4.15a. When the input pulse width is greater than the minimum pulse-width of the class-D stage, the RF-PWM is generated by the proposed architecture described in the previous section. When the pulse width is narrower than the minimum, the switched capacitors at the output stage are controlled by digital bits to control output power.

The output signal in a polar transmitter that employs a digital-to-analog converter in the output stage, using digital PAs, has quantization error

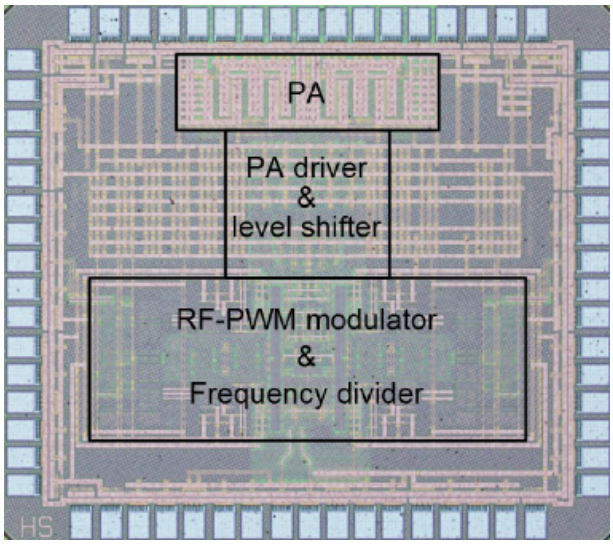


Figure 4.16: Die photograph

and also potentially a mismatch between the phase and the envelope. In the proposed solution, the impact of the mismatch is minimized due to self-alignment between the phase and envelope information. By partitioning the dynamic range between pulse-width and pulse-amplitude control, the hybrid solution also reduces the precision required of the amplitude control for a given output quantization noise floor level. As can be observed from the simulation result in Fig. 4.15b, a 4 bit control in the proposed hybrid architecture has a similar quantization noise floor as that generated by a 8 bit RF DAC based on a SCPA.

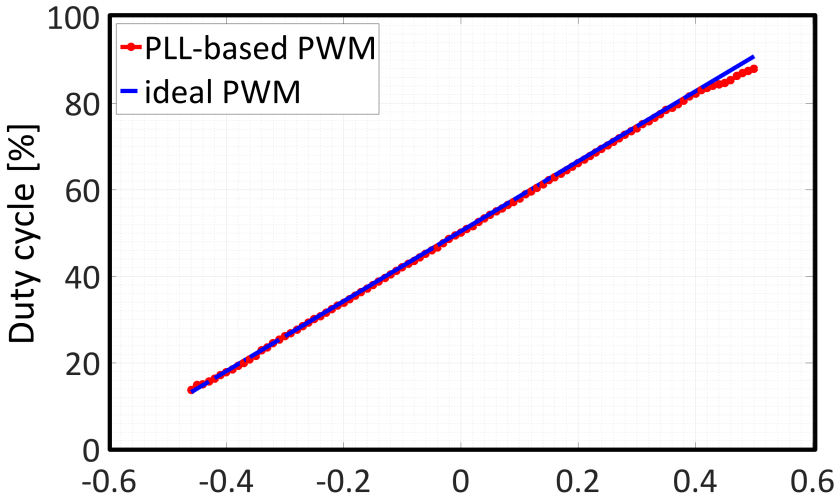
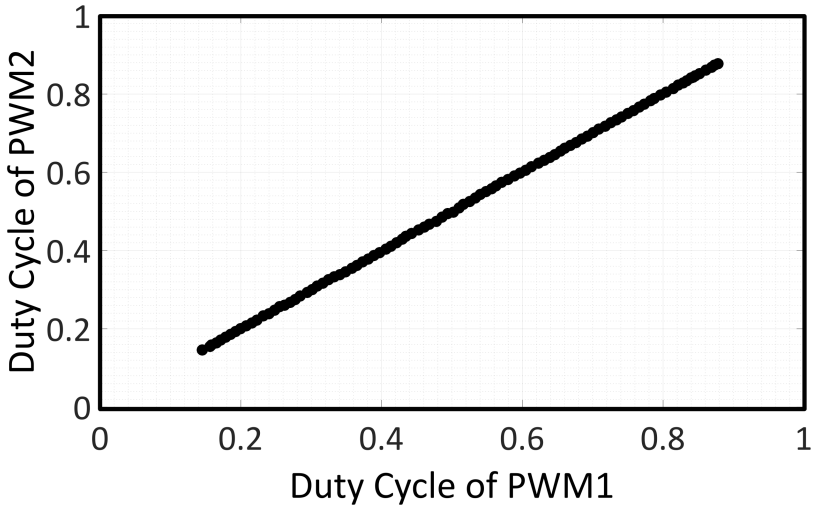


Figure 4.17: Measurement of duty cycle vs. input voltage

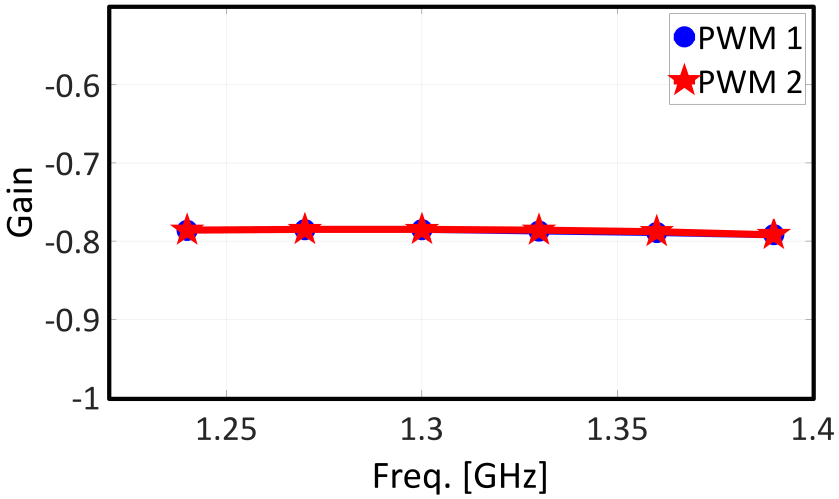
4.6 Measured Results

The design is implemented in a 65-nm CMOS process (Fig. 4.16) and uses an active area of 0.48 mm^2. The IC is measured on a four layer FR-4 printed circuit board and is housed in a QFN 48 package. The external matching includes an LC network for impedance transformation and a 1:1 balun for differential-to-single conversion on the board. The measured results are corrected for the losses in the off-chip network.

The linearity of each PLL-based pulse-width modulators is measured independently. As shown in Fig. 4.17, a linear relationship between input voltage and duty cycle is observed in each modulator. Fig. 4.18a shows the duty cycle values in the two modulators. The modulator provides a constant system gain over a 150-MHz range of carrier frequencies (Fig. 4.18b).



(a) Measured duty cycle of two PLL-based PWMs



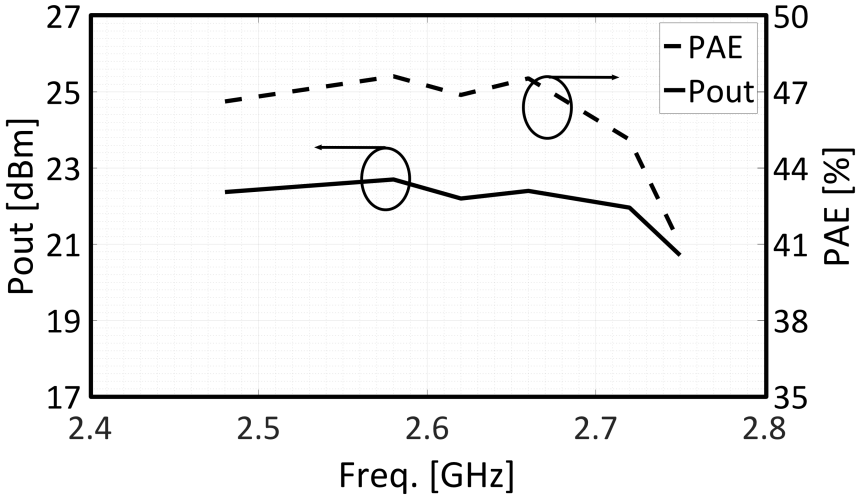
(b) Measured gain of two PLL-based PWMs

Figure 4.18: Measured performance of two PLL-based PWMs

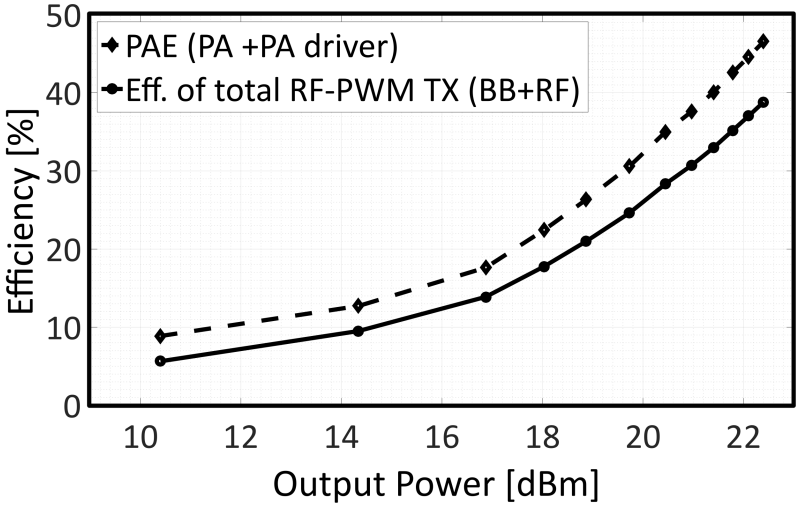
The PLL-based PWM employs a feedback loop with high gain and linearity performance. The two modulators are observed to match closely in measurement. The output linearity is observed to degrade for narrow pulse widths.

The external output matching network consists of discrete L-C components, bond wire inductance, and the 1:1 balun. The quality factor of the matching network is sufficiently low that it can provide good output power and PAE performance over a range of frequencies within approximately ±5% of the center frequency (2.66-GHz). The system exhibits 1 dB power deviation over 300-MHz (Fig. 4.19a). Fig. 4.20 shows the power level of the harmonics of f_{Ref}. The relative power levels of the 3^{rd} and 5^{th} order harmonics, which are closest to the fundamental RF output, are about 40 dB and 50 dB below the fundamental output power respectively.

The measured TX efficiency of the design including the PLL-based RF-PWM generator, level shifter, driver amplifier and PA, and the measured PAE, that includes the driver and the output stage, are shown in Fig. 4.19b. A peak PAE of 46.6% and peak total efficiency of 38.8% are observed at a carrier frequency of 2.66-GHz. With a 2.4 V supply, the power amplifier can provide a peak power output of 22.4 dBm. For a 1.4-MHz LTE signal with 6.4 dB PAR, the RF-PWM generator consumes 70-mW and the output stage including level shifters, PA drivers, and PAs consumes 230-mW. The average output power is 16.1 dBm for the PAE of 17.5%, an EVM of -24.9 dB, and ACLR of -30.9 dBc and -31.1 dBc. Fig. 4.21 shows the measured spectrum of

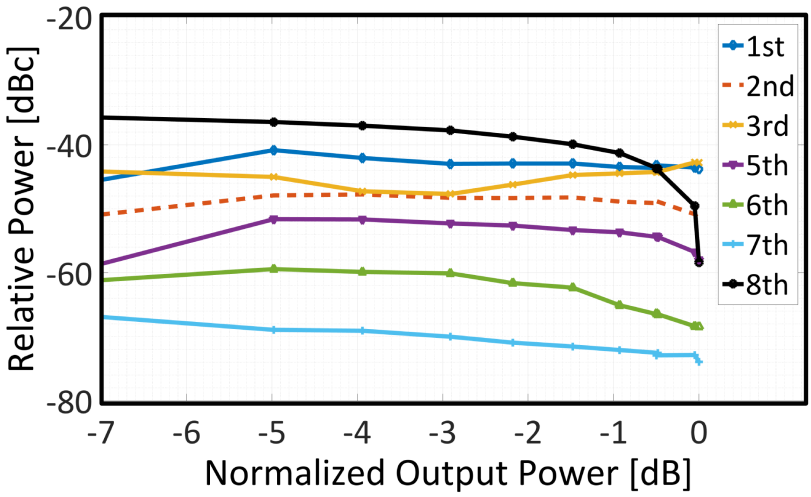


(a) Measured output power and PAE vs. frequency (at duty cycle =50%)

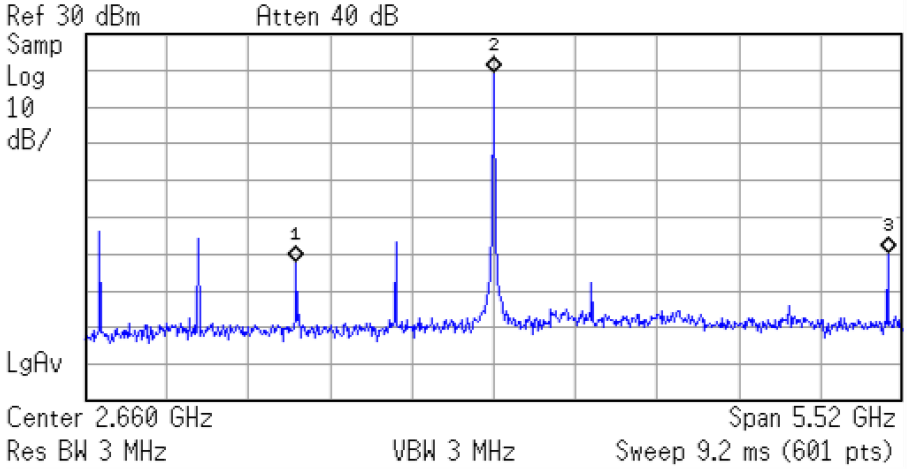


(b) Measured output power vs. PAE of PA stage and total system

Figure 4.19: Output power and efficiency



(a) Measured relative harmonic frequency power vs. output power (w/ varying duty cycle at f_{Ref} = 665-MHz)



(b) Measured output spectrum (full span = 5.52-GHz)

Figure 4.20: Measured relative harmonic power and the output spectrum (full span = 5.52-GHz)

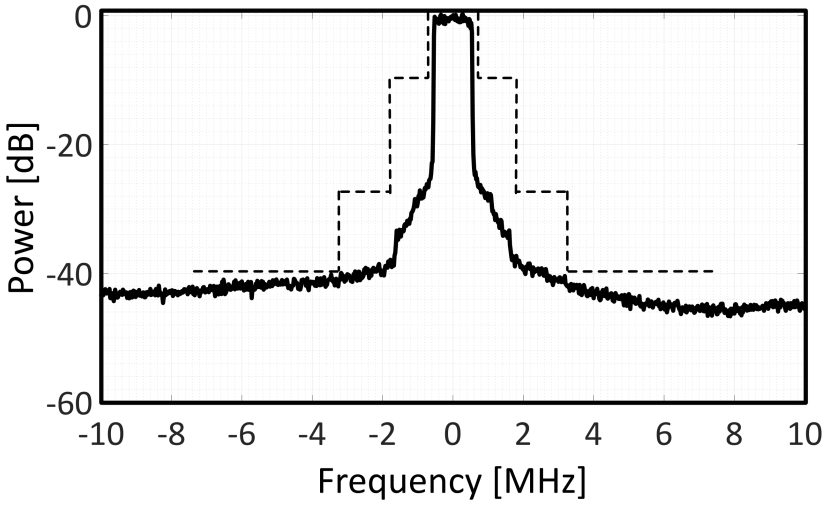


Figure 4.21: Measured output spectrum of LTE signal (RBW = 30-KHz)

the proposed transmitter.

Table. 4.1 shows a comparison of the CMOS RF transmitters utilizing switching PAs. The proposed design is observed to have the highest peak efficiency at highest carrier frequency relative to prior work.

4.7 Conclusion

This chapter presents a PLL-based RF-PWM transmitter with a Class-D power amplifier. The design is expected to be suitable for the LTE-MTC system, owing to its low complexity, cost, and high efficiency. The PWM output is combined with a Class-D output stage. Stacked Class-D amplifier stages allow operation at 2.4 V supply without excessive device voltage stress.

	[5]	[43]	[44]	[19]	This work
Carrier Freq.	2.2-GHz	2-GHz	800-MHz	750-MHz - 930-MHz	2.66-GHz
Supply vol.	2.5 V	1 V	1.1 V	1 V	1.2/2.4 V
Linearization Method	RF-PWM	RF-PWM	Digital I-Q	Digital Polar	RF-PWM
PA Class	E	No PA	SCPA	SCPA	D
Mod. signal	π/4-DQPSK symbol rate =192-KHz	16 QAM BW 5-MHz PAPR 6.9 dB	LTE BW 10-MHz PAPR 6.9 dB	64 QAM BW 1/2-MHz PAPR 8 dB	LTE BW 1.4-MHz PAPR 6.4 dB
Avg. P_{OUT}	26.7 dBm	-	6.97 dBm	0 dBm	16.1 dBm
Avg. PAE	21%[1)]	-	29.1%[2)]	14%[2)]	17.5%[1)]/13.4%[2)]
Peak P_{OUT}	28.6 dBm	-	13.9 dBm	8 dBm	22.4 dBm
Efficiency at $P_{OUT,peak}$	28.5%[1)]	-	40.4%[2)]	45%[1)]	46.6%[1)]/38.8%[2)]
Power cons. w/o PA	-	134-mW	-	3.3-mW	70-mW
E-UTRA ACLR	-	-	-32.4 dBc /-32.7 dBc	-	-30.9 dBc /-31.1 dBc
or EVM	-26.7 dB	-23.4 dB	-	-27.13 dB	-24.9 dB
Active area			0.24 mm^2	0.72 mm^2	0.48 mm^2
Technology	65-nm CMOS	40-nm CMOS	28-nm CMOS	40-nm CMOS	65-nm CMOS

[1)]PAE of the RF stage
[2)]PAE of the total system including baseband and RF stage

Table 4.1: Comparison Table

Chapter 5

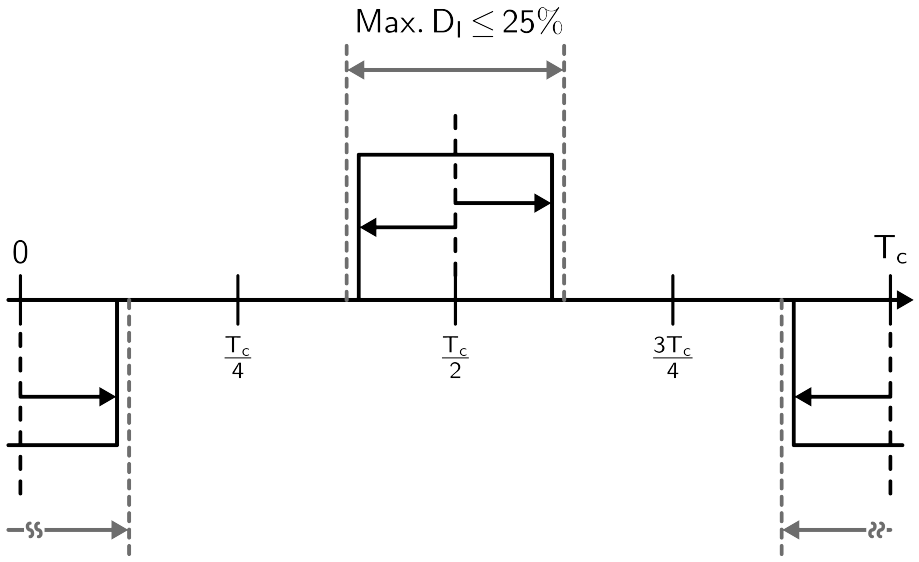
Cartesian PLL-Based RF-PWM[1] Transmitter

5.1 Introduction

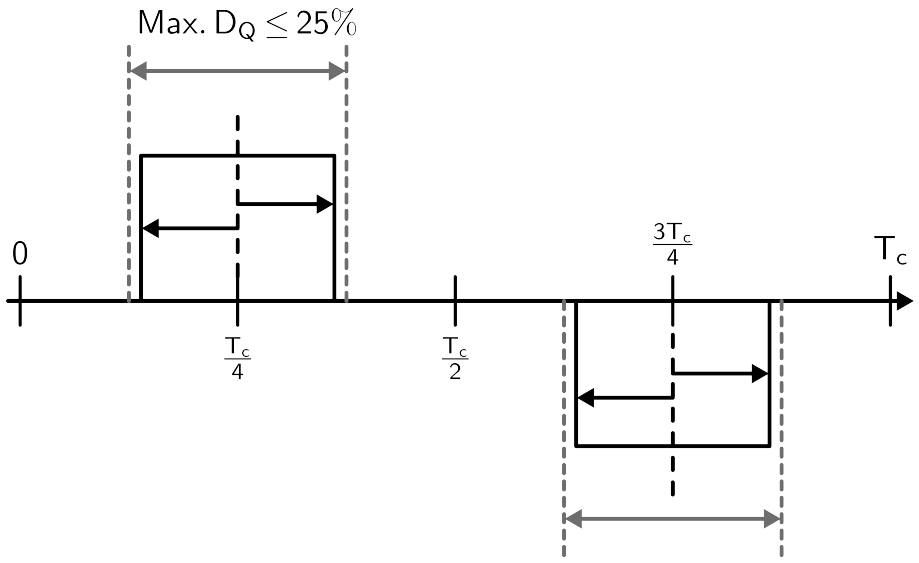
A transmitter architecture that employs three-level RF-PWM with a class-D output stage is described in this chapter. The design employs an input signal with a Cartesian format instead of a polar format at baseband. A Cartesian architecture is explored since it can potentially support wider bandwidth signals compared to a polar design. The RF output signal is generated without an upconverter, as in the polar design discussed earlier. The design uses two PWM generators, where each modulator produces a PWM signal whose duty cycle at a given instance corresponds to the instantaneous value of the I or Q input. For the power stage, a switched capacitor structure [23] is employed to provide a differential three-level RF-PWM signal with a conventional 2 port output stage. The architecture is simulated in a 65-nm CMOS process.

5.2 Cartesian Three-level RF-PWM Technique

[1]Part of the material in this chapter is based on [2] which has been published in IEEE DCAS 2016. The author Hyejeong Song designed and simulated the architecture.



(a) RF-PWM for I signal



(b) RF-PWM for Q signal

Figure 5.1: RF-PWM pulses for I and Q paths

The proposed modulation technique utilizes a center-aligned three-level RF-PWM signal (Fig. 5.1). This signal consists of a positive and a negative pulse, each with duty cycle (D) which is a linear function of the RF-PWM generator input (X_{IN}). In this signaling scheme, the time difference between the centers of two pulses is fixed to half of a period (T_c) of the carrier frequency. The width of the pulse is controlled by the input signal and changes symmetrically around the center of the pulse. A Fourier Series representation of the proposed RF-PWM signals is shown below.

$$\begin{aligned} V_{out,I}(t) &= \sum_{n=1}^{\infty} sgn\left(X_{IN,I}(t)\right) \frac{2V_{DD}}{n\pi} sin\left(2n\pi D_I\right) \\ &\quad \cdot \left(1 - cos(n\pi)\right) cos\left(\frac{2n\pi}{T_c} t\right) \end{aligned} \tag{5.1}$$

$$\begin{aligned} V_{out,Q}(t) &= (-1) \cdot \sum_{n=1}^{\infty} sgn(X_{IN,Q}(t)) \frac{4V_{DD}}{n\pi} sin(2n\pi D_Q) \\ &\quad \cdot sin\left(\frac{n\pi}{2}\right) sin\left(\frac{2n\pi}{T_c} t\right) \end{aligned} \tag{5.2}$$

The duty cycles D_I and D_Q, in the above equations, are proportional to the instantaneous magnitudes of the I and Q path baseband signals, respectively. Generation of the RF output signal without up-conversion is possible by pre-distorting the input signal using an inverse sine function (sin^{-1}) [3].

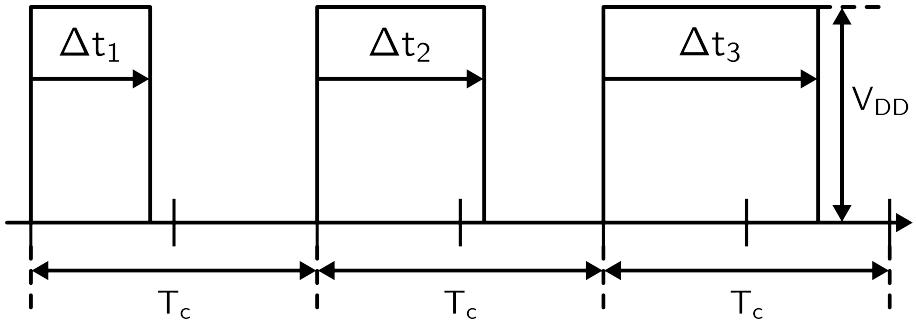


Figure 5.2: A conventional left-edge referred PWM signal

The maximum duty cycle of each pulse in the RF-PWM signal is 25%, and there is no overlap between the I and Q path signals. This makes it possible to share the output stage for I and Q signals, which improves the efficiency of the system.

As shown in Fig. 5.2, within a given period, a conventional left-edge referred PWM signal has a fixed rising edge position with a varying falling edge. The distance between the rising edges of two pulses is a period (T_c) of the PWM carrier frequency. The average of the modulated PWM signal has a linear relationship with input signal (Fig. 5.3) which is given by

$$\begin{aligned} D &= \frac{\Delta T}{T_c} \\ &= K_1 \cdot X_{IN}(t) + K_2 \end{aligned} \tag{5.3}$$

where D is the duty cycle of the pulse, K_1 is the constant gain of the PWM module, K_2 is the constant offset, and X_{IN} is the input signal. For instance,

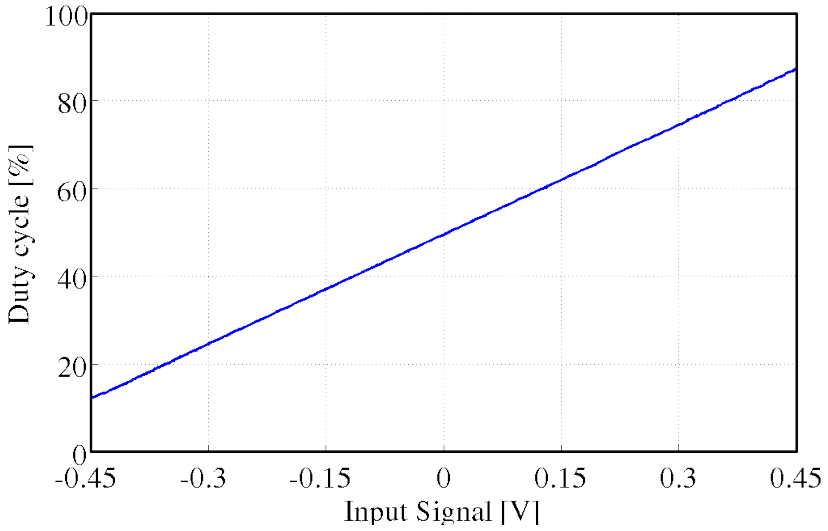
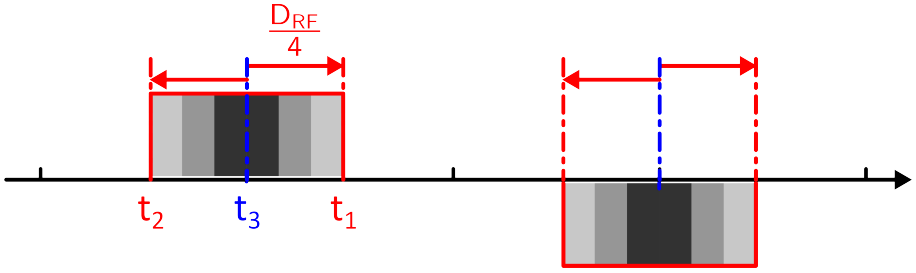


Figure 5.3: Input signal vs. duty cycle

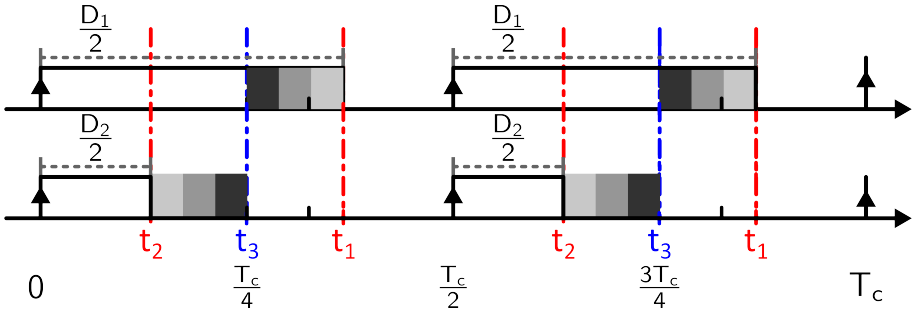
if the range of the input signal is $-A \leqq X_{In}(t) \leqq A$, K_1 is $1/(2A)$ and K_2 is 0.5.

As shown in Fig. 5.4, the proposed technique generates RF-PWM by using two modules that provide the PWM described in Eq. 5.3. In Fig. 5.4b, the rising edges of two pulses are aligned by using the same reference clock signal in two pulse-width modulators. Also, the falling edges (t_1 and t_2) represent the input signals ($X_{IN,1}(t)$ and $X_{IN,2}(t)$) respectively and are given by

$$t_1 = \frac{1}{2} \cdot D_1 \cdot T_c = \frac{1}{2} \{K_1 \cdot X_{IN,1}(t) + K_2\} \cdot T_c \tag{5.4}$$



(a) Cartesian RF-PWM



(b) RF-PWM generation using two PWM pulses

Figure 5.4: Cartesian RF-PWM pulse and PWM pulses

$$t_2 = \frac{1}{2} \cdot D_2 \cdot T_c = \frac{1}{2} \{K_1 \cdot X_{IN,2}(t) + K_2\} \cdot T_c \tag{5.5}$$

We can derive two control signals for the PWM modules by imposing the following conditions:

- The difference between the two generated pulse widths is the same as the pulse width of the desired RF-PWM pulse.

$$D_{RF} = 2 \cdot \frac{t_{1,m} - t_{2,m}}{T_{RF}} = K_1 \cdot X_{IN,PD,m}(t) + K_2, \qquad m = I \ or \ Q \tag{5.6}$$

- The center of two falling edges is aligned to the center of the RF-PWM pulse.

$$\frac{t_{1,m} + t_{2,m}}{2} = n \cdot \frac{T_{RF}}{4}, \qquad n = \begin{cases} 1 & for \ m = I \\ 2 & for \ m = Q \end{cases} \tag{5.7}$$

From Eq. 5.6 and Eq. 5.7, the two input control signals ($X_{IN,1,m}$ &$X_{IN,2,m}$) are given by

$$X_{IN,1,m} = \frac{1}{2}\left\{X_{IN,PD,m}(t) + \frac{K_2}{K_1}\right\} + \frac{n}{2K_1} - \frac{K_2}{K_1} \quad n = \begin{cases} 1 & for\ m = I \\ 2 & for\ m = Q \end{cases}$$

$$X_{IN,2,m} = -\frac{1}{2}\left\{X_{IN,PD,m}(t) + \frac{K_2}{K_1}\right\} + \frac{n}{2K_1} - \frac{K_2}{K_1} \quad n = \begin{cases} 1 & for\ m = I \\ 2 & for\ m = Q \end{cases} \tag{5.8}$$

$X_{IN,PD,I}(t)$ and $X_{IN,PD,Q}(t)$ are the pre-distorted input signals at baseband and are generated from $X_{IN,I}(t)$ and $X_{IN,Q}(t)$, respectively, which are the components of the original Cartesian input signal. From Eq. 5.1-Eq. 5.3, the pre-distorted input signals are given by

$$X_{IN,PD,m} = \frac{1}{2\pi K_1} sin^{-1}\left(\frac{\pi}{4V_{DD}} \cdot X_{IN,m}\right) - \frac{K_2}{K_1} \quad ,\ m = I\ or\ Q \tag{5.9}$$

The proposed RF-PWM generator is shown Fig. 5.5. In order to produce two pulses in a single RF period, the switching frequency is made twice that of the target RF frequency. In the pre-distortion block, the input signal is used to generate two signals in the quadrature paths, namely, $X_{IN,I1}$ and $X_{IN,I2}$ in the I-path, and $X_{IN,Q1}$ and $X_{IN,Q2}$ in the Q-path. These signals are converted into two baseband PWM signals from which the RF-PWM signal is derived. Two reference clocks (CLK_I and CLK_Q) with a relative phase-

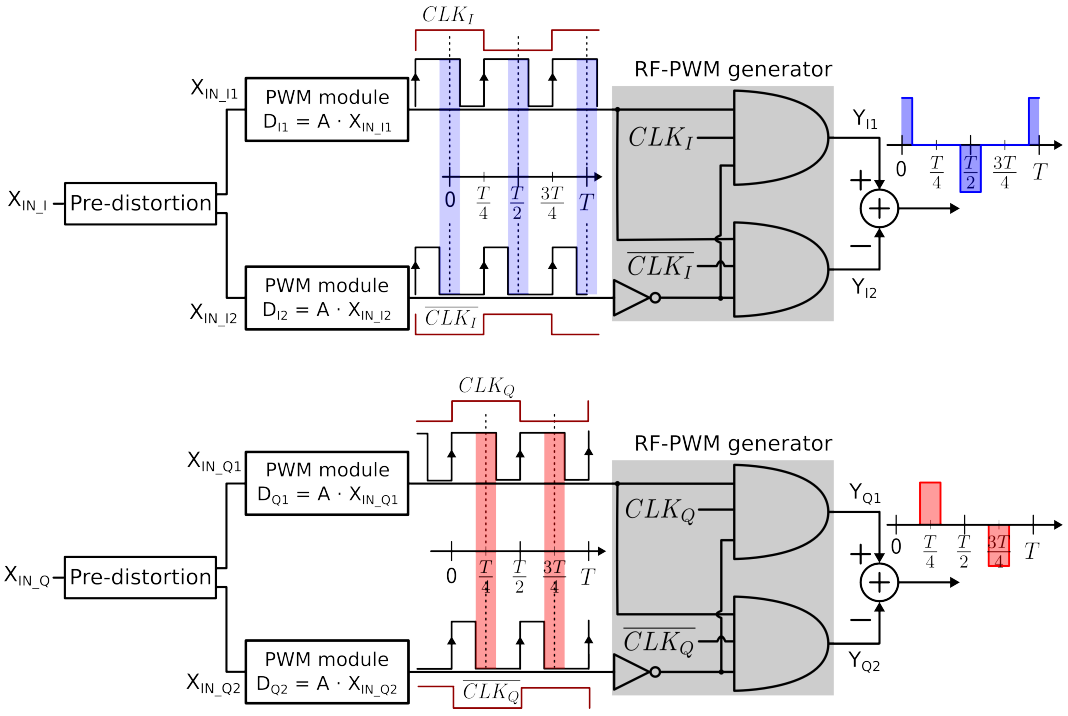


Figure 5.5: RF-PWM generation system

shift of 90° can be used to provide I-Q modulation. In addition, in order to accommodate a negative input signal a differential architecture is utilized.

For an RF-PWM generator, it is necessary to design a PWM generator which operates at RF. This is a major challenge if a PWM module based on an analog ramp generator and comparator is employed. For this technique, a PLL-based pulse-width modulator [37, 38] which operates at GHz frequencies is employed. The output of the phase detector (PD) in the PLL provides a PWM signal which is proportional to the phase difference between the reference clock and the output of VCO. The phase difference is controlled by the input signal because the feedback loop forces the local average of the difference between the PWM signal at the output of the phase detector and the input to be a zero. The pulse-width modulator provides two pulses per RF period since two comparisons are performed in a single period. The carrier frequency of the RF-PWM is equal to the frequency of the reference clock. The PWM generator can be used to provide I-Q output signals by using reference clocks with 90° phase shift. It also allows for the system to operate over multiple bands, which can be accomplished by changing the reference clock. In the proposed architecture which employs PLL-based PWM (Fig. 5.6), the VCO signal and the reference clock signal are compared twice per period because an EX-OR is used as the phase detector. Due to this, a pulse signal is generated with a time period of $0.5T_c$, and the duty cycle (D) of each pulse is half of the original duty cycle, which can be calculated from Eq. 5.3. These two pulses are directly used for three-level PWM which consists of two pulses with

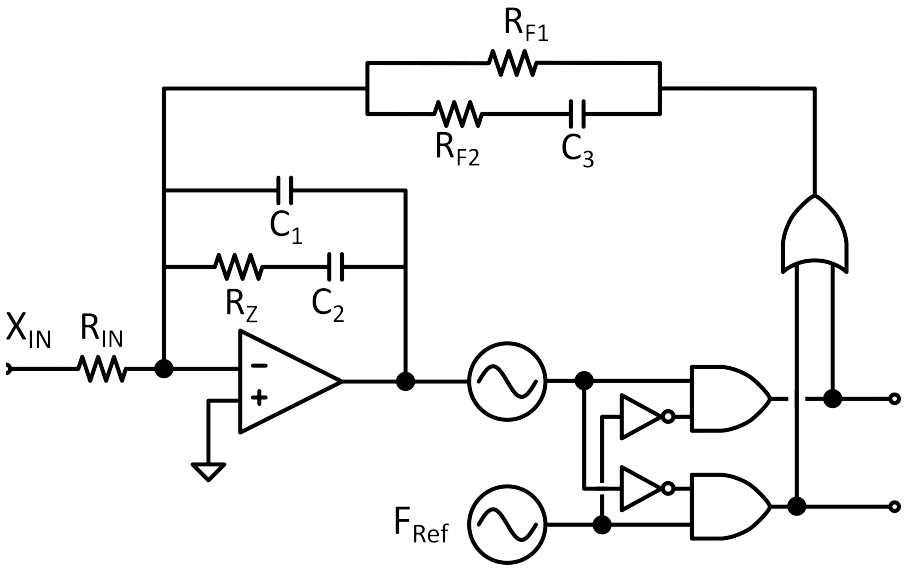
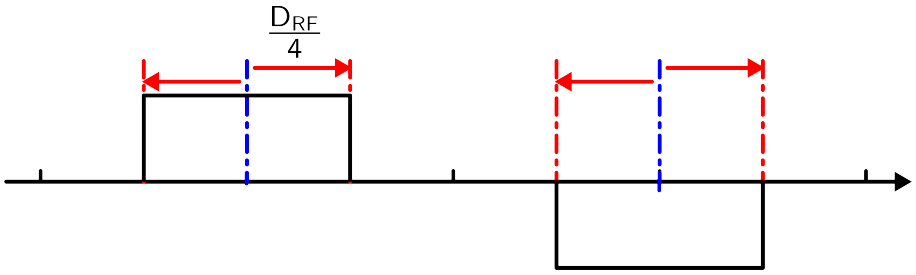


Figure 5.6: The proposed PLL-based PWM generator

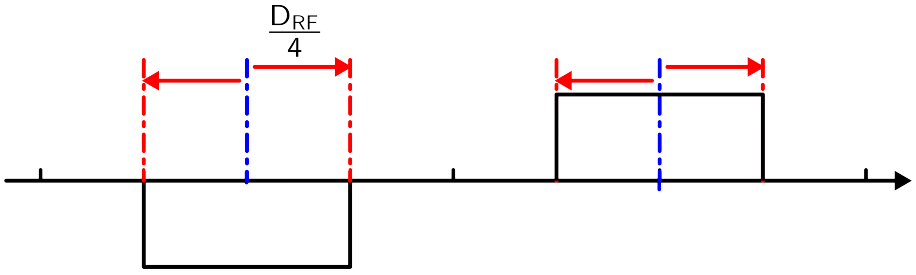
a relative phase-shift of 180°. This technique faces an issue of representing negative values with the duty cycle because the output is the ratio between the pulse width and the period of the PWM signal. As shown in Fig. 5.7, negative values of the input signal are obtained utilizing an inverted RF-PWM signal.

5.3 Analysis of the Proposed Architecture

The circuit blocks of the proposed Cartesian RF-PWM transmitter are shown in Fig. 5.5. In order to analyze the architecture, linearized models for each blocks, which were introduced in the chapter 3, are employed. A key difference is that the EX-OR phase detector is modified due to the use of 3-level RF-PWM (Fig. 5.6), which requires the use of a different model.



(a) RF-PWM pulse with a positive input signal



(b) RF-PWM pulses as $X_{IN} = (-1) \cdot |X_{IN}|$

Figure 5.7: RF-PWM pulses for a positive and a negative input signal

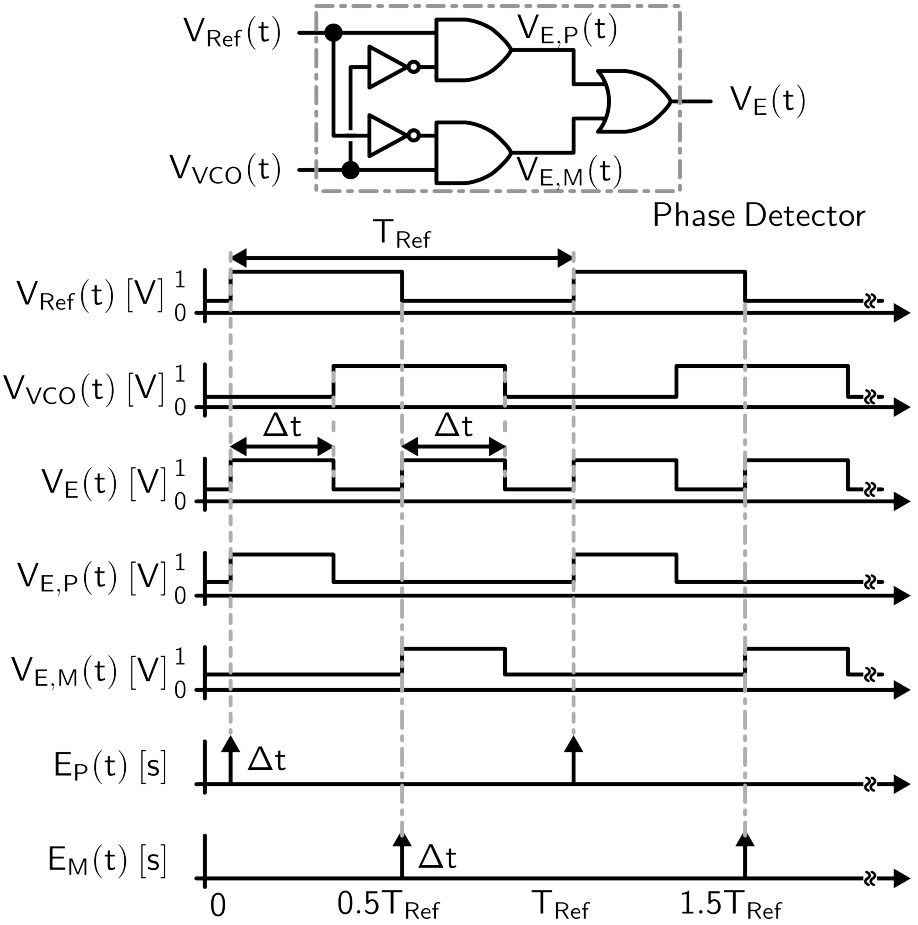


Figure 5.8: EX-OR phase detector and associated signals.

5.3.1 Linearized Model of the EX-OR Phase Detector

For the analysis of the proposed Cartesian RF-PWM transmitter architecture, it is necessary to develop linearized frequency domain models for each sub-block. In the previous chapter, a model of the EX-OR phase detector is proposed to analyze both the baseband signal and the signals located

at higher frequencies. For the architecture here, it is necessary to modify the model because the output of the phase detector ($V_E(t)$) consists of two signals ($V_{E,P}(t)$ and $V_{E,N}(t)$) which are transmitted through a separated path, and generate three-level RF-PWM outputs. The subscript P and N denote the positive pulse and the negative pulse, respectively. Fig. 5.8 depicts an EX-OR phase detector and its associated signals. As described in the chapter 4, a simplification of $V_{E,P}(t)$ and $V_{E,M}(t)$ by a sequence of impulse trains weighted by the pulse width (Δt) can be employed since the signal information is encoded in the pulse width rather than the actual voltage shape [39].

The impulse sequences ($E_{P,1}(t)$, $E_{M,1}(t)$, $E_{P,2}(t)$, and $E_{M,2}(t)$) can be defined as

$$\begin{aligned} E_{P,m}(t) = &\quad \Delta t_m(t) \cdot \textstyle\sum_{n=-\infty}^{\infty} \delta\left(t - n \cdot T_{Ref}\right) \\ E_{M,m}(t) = &\quad \Delta t_m(t) \cdot \textstyle\sum_{n=-\infty}^{\infty} \delta\left(t - n \cdot T_{Ref} - \dfrac{T_{Ref}}{2}\right) \end{aligned}, \qquad m = 1,\ 2 \quad (5.10)$$

VCO frequency variations are not significant in a time window that is short compared to the inverse of the signal bandwidth in the locked state, since the bandwidth of the input signal is about two orders of magnitude lower than the reference frequency. By using Eq. 5.3, the relationship of Δt to the phase difference ($\phi_E(t)$) can be approximated by

$$\begin{aligned} \Delta t_m(t) &= T_{Ref} \cdot \frac{D_m(t)}{2} \\ &\approx \frac{T_{Ref}}{2\pi}\phi_{E,m} \end{aligned} \quad , \qquad m = 1\,or\,2 \tag{5.11}$$

where ϕ_E denotes the phase difference between the VCO output and the reference signal, and the subscript m signifies the index of each PLL-based pulse-width modulators. Combining Eq. 5.10 and Eq. 5.11, the pulse width of the output signals of the modulator can be approximately modeled as

$$\begin{aligned} E_{m,P}(t) &= \frac{T_{Ref}}{2\pi} \cdot \phi_{E,m}(t) \cdot \textstyle\sum_{n=-\infty}^{\infty} \delta\left(t - \frac{T_{Ref}}{2}n\right) \\ E_{m,\mathrm{M}}(t) &= \frac{T_{Ref}}{2\pi} \cdot \phi_{E,m}(t) \cdot \textstyle\sum_{n=-\infty}^{\infty} \delta\left(t - \frac{T_{Ref}}{2}n - \frac{T_{Ref}}{2}\right) \end{aligned} \quad , \qquad m = 1\,or\,2 \tag{5.12}$$

Fig. 5.9 illustrates the resulting model of the phase detectors. As with the model in chapter 4, the baseband components $Y(t)$ are utilized for analysis of the PLL-based pulse-width modulator and pulse width sequences $E_{m,P}(t)$ and $E_{m,N}(t)$ are utilized for analysis of the RF-PWM generator.

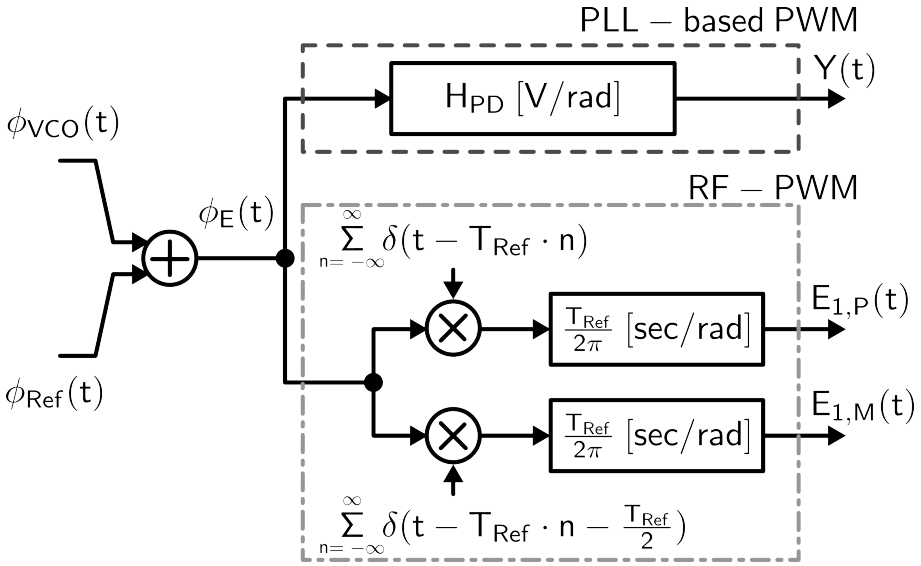


Figure 5.9: Linear model of the EX-OR phase detector.

5.3.2 Linear Model of the RF-PWM Generator

Fig. 5.10 illustrates the linear model of the RF-PWM generators. The RF modulator consists of four EX-OR and two OR gates, where the I-Q information ($X_{I,IN}(t)$ and $X_{Q,IN}(t)$) is encoded in the duty cycles $D_{RF,I}$ and $D_{RF,Q}$. The EX-OR function detects the difference and the mid-point of the falling edges of the two input PWM signals, and the OR function combines the I-Q PWM signals.

The frequency response of the signal (Δt_m) that is sampled with period $T_{Ref}/2$ can be found by taking the Fourier Transform of Eq. 5.12, which leads to

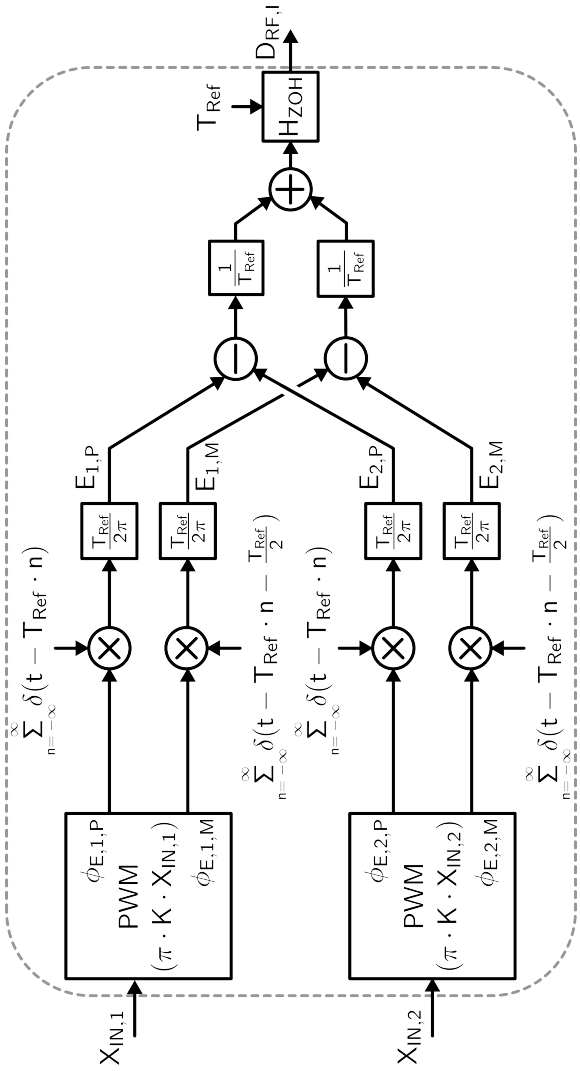


Figure 5.10: Linear model of EX-OR phase detector.

$$
\begin{aligned}
E_{m,\mathrm{P}}(j\omega) = &\quad \frac{1}{T_{Ref}} \sum_{k=-\infty}^{\infty} \frac{T_{Ref}}{2} \cdot K \cdot X_m \left(j\omega - \frac{2\pi n}{T_{Ref}} \right) \\
E_{m,\mathrm{M}}(j\omega) = &\quad \frac{1}{T_{Ref}} \sum_{k=-\infty}^{\infty} \frac{T_{Ref}}{2} \cdot K \cdot X_m \left(j\omega - \frac{2\pi n}{T_{Ref}} \right) \cdot e^{j\frac{T_{Ref}}{2}\omega}
\end{aligned}
\quad , \; m = 1, \; 2 \tag{5.13}
$$

The EX-OR phase detector encodes the duty cycle and phase information into a pulse, which can be separately modeled by linear addition and subtraction with corresponding constant gains.

We employ an impulse approximation to analyze the logic functionality of RF-PWM generator. To further analyze the analog RF output noise, we need to convert signals from the discrete-time domain to the analog domain. By applying a zero-order-hold reconstruction filter with a sampling time of $T_{REF}/2$, we can transfer signal analysis from discrete-time to analog. The duty cycle and the phase offset of RF-PWM can be formulated in the analog domain as

$$
\begin{aligned}
D_{i,P}(j\omega) &= \frac{K_1}{2} \cdot \{X_{IN,i,1}(j\omega) - X_{IN,i,2}(j\omega)\} \\
D_{i,N}(j\omega) &= \frac{K_1}{2} \cdot \{X_{IN,i,1}(j\omega) - X_{IN,i,2}(j\omega)\} \quad , \qquad i = I, \; Q \\
D_{RF,i}(j\omega) &= D_{i,P}(j\omega) + D_{i,N}(j\omega) \\
&= K_1 \cdot \{X_{IN,i,1}(j\omega) - X_{IN,i,2}(j\omega)\}
\end{aligned}
\tag{5.14}
$$

5.3.3 Noise Analysis of the RF-PWM Generator

Based on the Cartesian RF-PWM output at the carrier frequency (Eq. 5.1~5.2), the RF carrier harmonic for the RF-PWM with noise can be derived as

$$\begin{aligned} V_{out}(t) + N(t) &= \frac{4V_{DD}}{\pi} sin\left(\pi \left\{D_{I,RF}(t) + D_{N,I}\right\}\right) cos(2\pi f_c t) \\ &\quad - \frac{4V_{DD}}{\pi} sin\left(\pi \left\{D_{Q,RF}(t) + D_{N,Q}\right\}\right) sin(2\pi f_c t) \end{aligned} \tag{5.15}$$

We can perform a Taylor series expansion for given nominal I and Q duty cycles $D_{RF,I}$ and $D_{RF,Q}$, which can be formulated as

$$\begin{aligned} V_{out}(t) + N(t) &\approx \frac{4V_{DD}}{\pi} sin\left(\pi D_{I,RF}(t)\right) cos(2\pi f_c t) \\ &\quad - \frac{4V_{DD}}{\pi} sin\left(\pi D_{Q,RF}(t)\right) sin(2\pi f_c t) \\ &\quad + \frac{4V_{DD}}{\pi} cos\left(\pi D_{I,RF}(t)\right) \cdot \pi \cdot D_{N,I} \cdot cos(2\pi f_c t) \\ &\quad - \frac{4V_{DD}}{\pi} cos\left(\pi D_{Q,RF}(t)\right) \cdot \pi \cdot D_{N,Q} \cdot sin(2\pi f_c t) \end{aligned} \tag{5.16}$$

The total spectral noise power ($S_{N(t)}(j\omega)$) can be derived employing

the method introduced in 4.3.5, and can be shown to be proportional to the RF-PWM phase error spectral noise power ($S_{N_{\phi_E}}(j\omega)$) as shown below.

$$S_{N(t)}(j\omega) = \frac{1}{2}\left(\frac{4V_{DD}}{\pi}\right)^2 \cdot 4S_{N_{\phi_E}}(j\omega) \tag{5.17}$$

where we assume that individual phase error noise power injected from all EX-OR phase detectors is identical. The noise of RF-PWM is thus a total sum of RF-PWM phase noise contributions. Consequently, as in the polar design, the in-band and out-of-band noise are strongly dependent on the analog filter and VCO noise, respectively.

5.4 Power Amplifier Stage

The architecture of the proposed PA stages is shown in Fig. 5.11. It includes logic gates for combining the I-Q signals, level shifters, PA drivers, switched capacitor PAs and a bandpass matching network. The combining of the I-Q signals is possible before the PA stage by using logic gates, and the PA stages can be shared because the maximum duty cycle of each pulse is less than 25%. Also, the design allows for three-level PWM signal to be generated at the output by using a simple combiner such as a balun.

A stacked inverter structure is used in the PA design in order to achieve a large output power [33]. The design includes a level shifter which interfaces

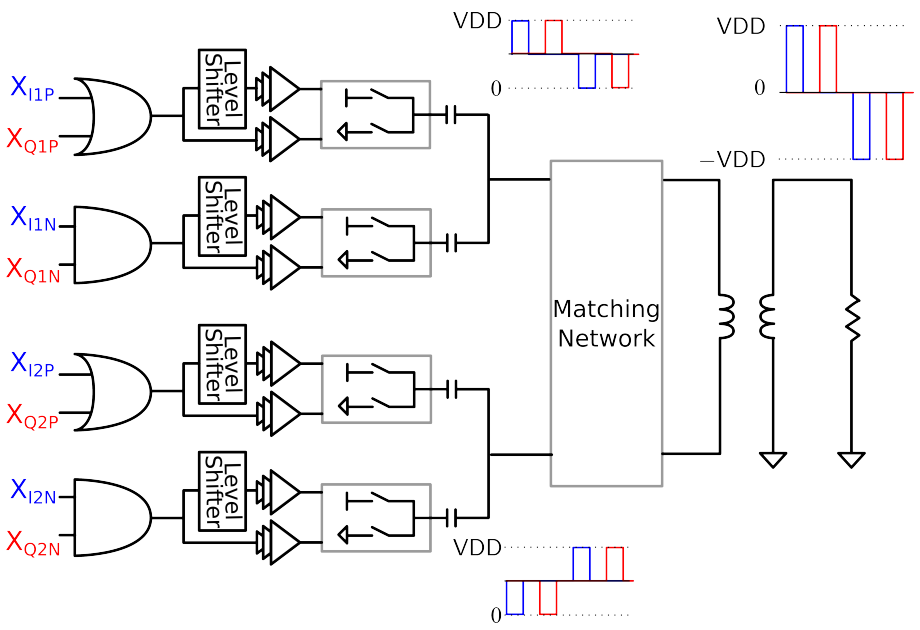


Figure 5.11: PA stage with a switched capacitor output

the RF-PWM signal to the cascode output stage. A key challenge in the design of class-D PAs, especially at high frequencies, arises from shoot-through currents. These currents appear when both the pull-up and pull-down devices in the class-D stage are simultaneously on, which can cause a significant degradation in efficiency. In order to address the shoot-through issue, we employ a separate PA driver for the PMOS and NMOS devices, which converts the RF-PWM signal into non-overlapping control signals by controlling the rise and fall times.

In order to mitigate the impact of bond-wire parasitics and common mode noise four PAs are utilized, which achieves differential PA outputs with three levels. However, it is difficult to combine four differential PA output

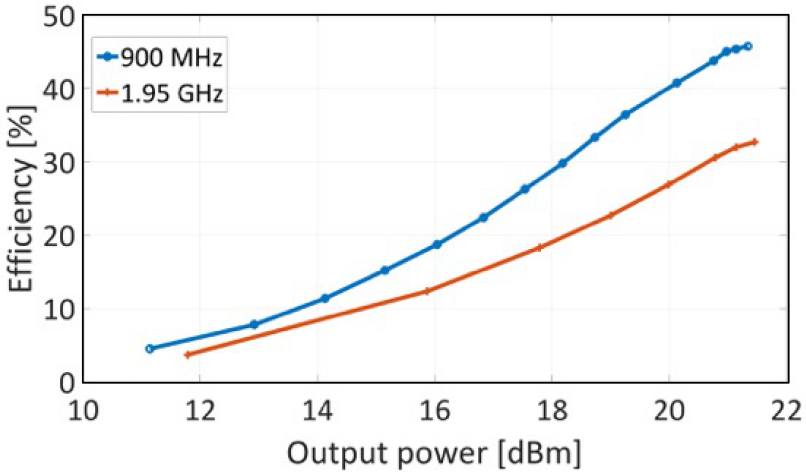
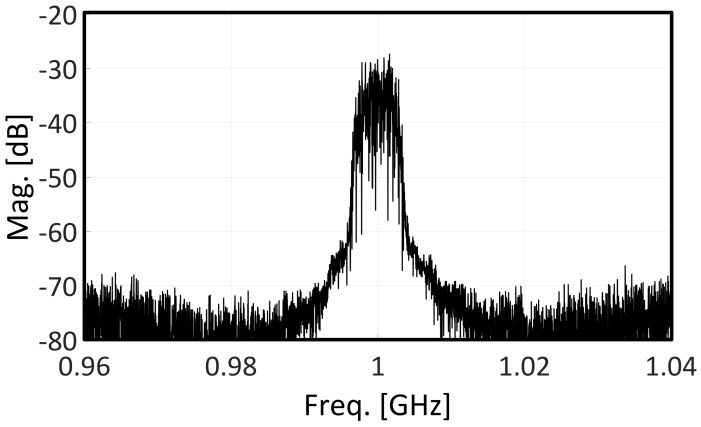


Figure 5.12: Output power vs Power Added Efficiency (PAE)

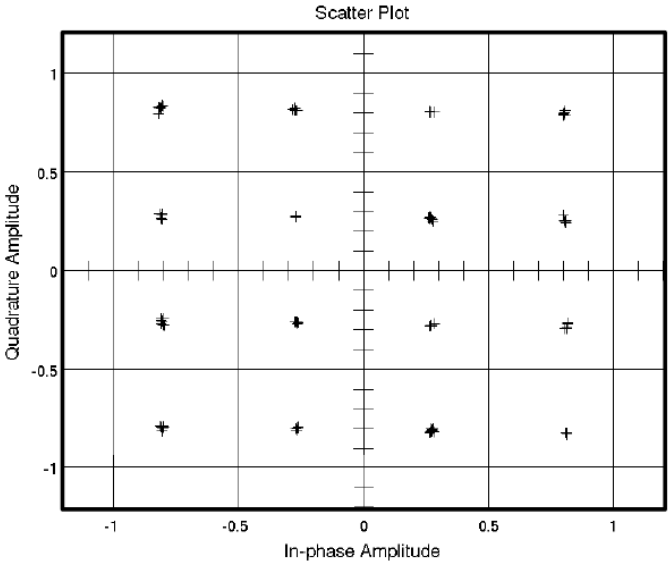
ports with conventional combiners. Therefore, we employ a switched capacitor technique to simplify the complexity of the PA stage [23]. To achieve the optimal load impedance and single-ended output signal with three levels, a matching network with a balun or a broadband transformer with the desired turns ratio was employed.

5.5 Simulation Results

The proposed RF-PWM transmitter has been designed and simulated in a 65-nm CMOS technology. The relationship between the input signal and the duty cycle of PWM signal is observed to be linear (Fig. 5.3). Also, the simulated efficiency of the design with the level shifter, driver amplifier and PA is shown in Fig. 5.12. A peak PAE of 48% is observed at 900-MHz and



(a) Output spectrum



(b) Constellation diagram

Figure 5.13: Output constellation for 16 QAM signal

33% at 1.95-GHz. With a 2.4 V supply, the power amplifier can provide a peak power output of approximately 22 dBm for both carrier frequencies with an unmodulated sine-wave output. The loss of the output matching network is assumed to be 1.3 dB.

A macromodel-based simulation of the transmitter employing a 16 QAM signal with 5-MHz bandwidth, with a carrier frequency at 900-MHz is shown in Fig. 5.13.

5.6 Conclusion

A Cartesian three-level RF-PWM transmitter based on a PLL-based PWM is proposed. A Class-D amplifier has been used as the output stage in order to enhance efficiency as shown by Fig. 5.12. The proposed architecture is digitally intensive and can be employed over multiple bands by changing the reference clock.

Chapter 6

Conclusion and Future Work

Three different PWM architectures, namely, PLL-based PWM, polar RF-PWM, and Cartesian 3-level RF-PWM, have been discussed for the design of high-efficiency wireless transmitters.

A polar RF-PWM transmitter has been proposed for use in IoT applications. A linear model for the proposed system and its noise analysis are presented. A prototype IC is implemented in a 65-nm CMOS process which achieved a peak PAE of 46.6% and peak total transmitter efficiency of 38.8% at a carrier frequency of 2.66 GHz with 22.4 dBm peak output power. When measured with a 1.4 MHz LTE signal and with 6.4 dB PAR, the average output power is 16.1 dBm with an average PAE of 17.5%.

The proposed Cartesian RF-PWM transmitter can handle wider signal bandwidths and uses 3-level RF-PWM. Due to 25% maximum pulse width for the I and Q components in the RF-PWM signal, the output PA stage can be shared between these components. The combined paths can provide the same maximum output power as the polar architecture. The simulation of the design in a 65-nm CMOS process yields peak PAE of 48% and 33% at 900 MHz and at 1.95 GHz, respectively. The peak output power in simulation is

observed to be 22 dBm at both carrier frequencies.

The RF-PWM transmitter architecture can achieve high efficiency since it directly drives a switch-mode PA, which enhances the overall efficiency in wireless modulation schemes with high PAPR such as OFDM. In addition, there is no quantization noise in this approach, since RF-PWM is generated in the analog domain. Since the design is switch-based, it can benefit from process scaling.

The modulators directly generate the output signal without up-converters, and the output frequency is determined by the reference clock in the PLL. The output carrier frequency can be varied over a wide range by controlling the reference frequency.

The design presented here employed a ring oscillator topology. As discussed in prior chapters, the out-of-band noise of the architectures is strongly dependent of the distant noise of the VCOs. Thus to enhance noise performance, the use of low-noise L-C based VCO topologies can be investigated.

The dynamic range of the RF-PWM transmitter is determined by the minimum pulse width that can be transmitted by the Class-D PA. Future work can explore the use of discrete amplitude control (chapter 4) for pulse widths that are narrower than a minimum limit for both the polar and the Cartesian designs.

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Vita

Hyejeong Song received the Bachelor of Science degree in Engineering from Kyungpook National University (KNU), Daegu, South Korea in 2006 and the Master of Science degree in Electrical Engineering from Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2008 in South Korea. The thesis title for her master's degree was "A Study on the Low Noise Amplifier for SDR". She started her Ph.D. program at the University of Texas (UT) at Austin in 2010.

Her doctoral research addresses the design and analysis of high efficiency CMOS wireless transmitters.

She has held internship positions at Samsung Telecommunication America, Texas Instruments Incorporated, and Intel. She has multiple publications in the area of radio-frequency integrated circuits and was a finalist in the Best Student Paper Award at IEEE RFIC Symposium, 2015.

Permanent address: hyejeongss@gmail.com

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